Name: _____ ID# _____

Date Submitted: _____ Lab Section # _____

CSE 2441 – Introduction to Digital Logic Fall Semester 2012

**Lab Number 7 -- An Introduction to Flip Flops**

**100 Points**

(To be performed the week of October 22, 2012)

**CSE 2441** **LABORATORYSESSION 7** **Fall 2012**

# AN INTRODUCTION TO FLIP-FLOPS

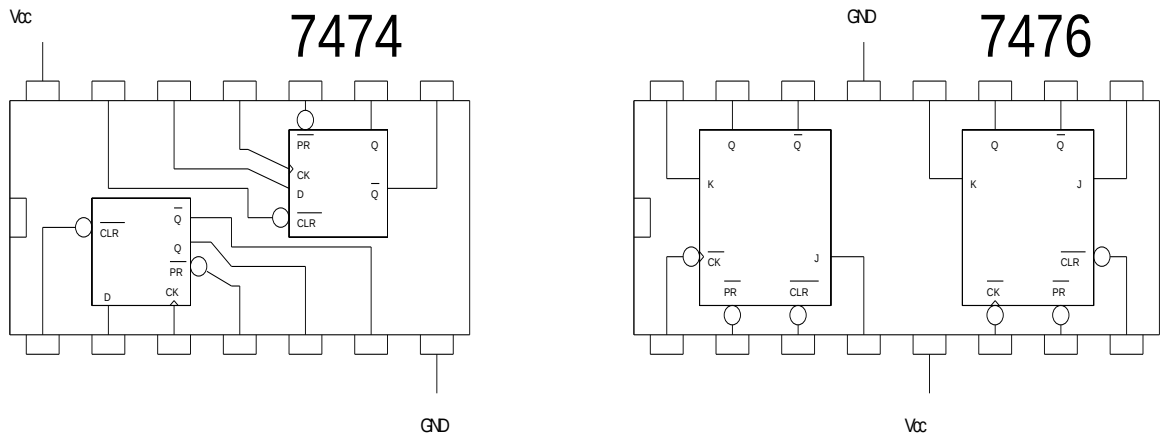
## (100 POINTS)

### PURPOSE/OUTCOMES:

To study the logical characteristics of type D and type J-K flip-flops and their use in basic shift registers and counters. After completing this laboratory, you'll have an understanding of how D and JK flip-flops work and be able to design basic registers and counters.

### BACKGROUND:

Flip-flops and latches are used as memory devices in sequential logic circuits. The D and JK flip-flop are the most commonly used flip-flops in synchronous sequential circuits. The figures below show pin-out diagrams for SN7474 and SN7476 implementations of D and JK filp-flops, respectively. Note that each package contains two flip-flops and that each flip-flop has data inputs, D or JK, clock inputs, clear and preset inputs, and complementary outputs.




### PROCEDURE:

Complete each of the exercises detailed below, and record your results and answers in your laboratory notebook. Have the lab instructor check your work after each part.

#### Part 1 – Learn the functionality of an SN7474 D Flip-flop.

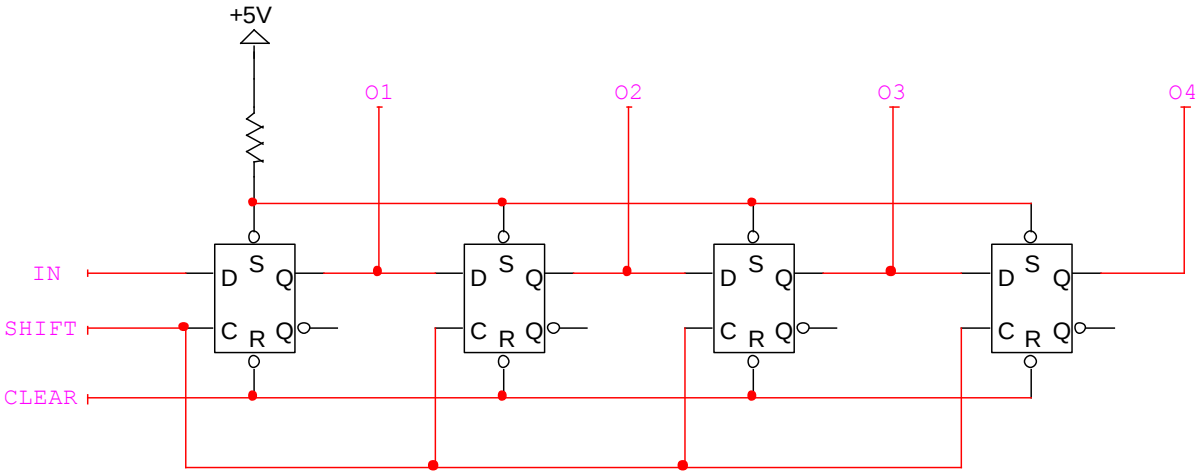
Experimentally derive the state table of an SN7474 D flip-flop. Include the D, CK, PR, and CLR inputs in your table. Use Pulse Switch A of the IDL-800 to drive the clock (CK) input of the 7474.

#### Part 2 – Learn the functionality of an SN7476 JK Flip-flop.

Experimentally derive the state table of an SN7476 JK flip-flop. Include the J, K, CK, PR, and CLR inputs in your table. Use Pulse Switch A of the IDL-800 to drive the clock (CK) input of the 7476.

**Part 3 – Implement a Basic Shift Register on the IDL 800 Using D Flip-flops.**

a. Complete construction of the circuit shown below.
b. The circuit that you constructed is a simple 4-bit, serial-in, serial/parallel-out shift register. Develop a procedure for testing the circuit.
c. Experimentally verify the functioning of the circuit using your test procedure.




**Part 4 – Implement a Four-Bit Twisted Ring Counter on the IDL 800.**

A four-bit twisted-ring counter can be realized from the circuit constructed above by connecting the complemented output of the last stage flip flop to the D input of the first stage.

a. Make the connection described above.
b. Place the shift-register in the all-0 state. Then experimentally derive the state sequence of the circuit, i.e., 0000 → 1000 → 1100 → 1110 → 1111 → … . List the complete sequence.
c. Place the shift-register in a state not found in the sequence observed above.
d. Experimentally verify the state sequence that results from this starting state. Record your results.
e. Which of the above sequences represents the state sequence of a twisted-ring counter?
**f.** How many states does an *n*-bit twisted-ring counter have?