Name: _____ ID# _____

Date Submitted: _____ Lab Section # _____

CSE 2441 – Introduction to Digital Logic Spring Semester 2013

Lab Number 7 – **An Introduction to Synchronous Circuits**

100 Points

(To be performed the week of March 18, 2013)

CSE 2441 **LABORATORYSESSION 7** **Spring 2013**

AN INTRODUCTION TO SYNCHRONOUS CIRCUITS

(100 POINTS)

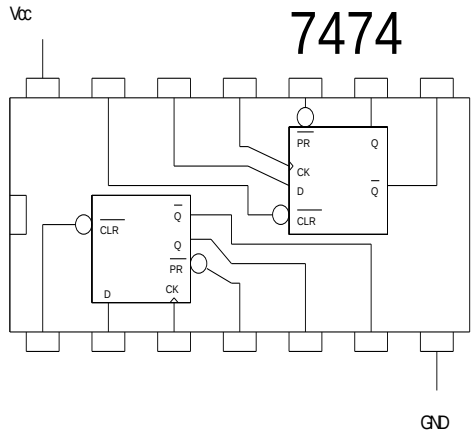
PURPOSE/OUTCOMES:

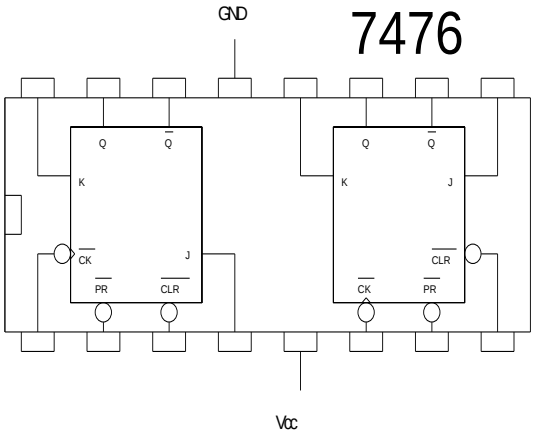
To study the functional characteristics of type D flip-flops and their use in basic shift registers and counters. After completing this laboratory, you'll have an understanding of how D flip-flops work and be able to analyze basic registers and counters.

BACKGROUND:

Flip-flops and latches are used as memory devices in sequential logic circuits. The D and JK flip-flop are the most commonly used flip-flops in synchronous sequential circuits. The figures below show pin-out diagrams for SN7474 and SN7476 implementations of D and JK filp-flops, respectively. Note that each package contains two flip-flops and that each flip-flop has data inputs, D or JK, clock inputs, clear and preset inputs, and complementary outputs.

This lab will focus on D flip-flops and basic registers and counters. JK flip-flops will be studied in later lab assignments.





PROCEDURE:

Complete each of the exercises detailed below, and record your results and answers in your laboratory notebook. Have the lab instructor check your work after each part.

Part 1 – Learn the functionality of an SN7474 D Flip-flop.

Experimentally derive the state table of an SN7474 D flip-flop. See the table format below. Use the following pin assignments when connecting the 7474 to the IDL-800.

D (pin 2) – SW7
PR (*pin 4*) – SW1
Q (pin 5) – LED7
Power (pin 14) – +5 V
CK (*pin 3*) – PULSE SWITCH A
CLR (pin 1) – SW0
Q' (pin 6) – LED 6
Ground (*pin 7*) – GND

D	***CK***	***PR***	***CLR***	***Q***	***Q****
d	↑	1	0	0	
d	↑	1	0	1	
d	↑	0	1	0	
d	↑	0	1	1	
d	↑	0	0	0	
d	↑	0	0	1	
0	↑	1	1	0	
0	↑	1	1	1	
1	↑	1	1	0	
1	↑	1	1	1	

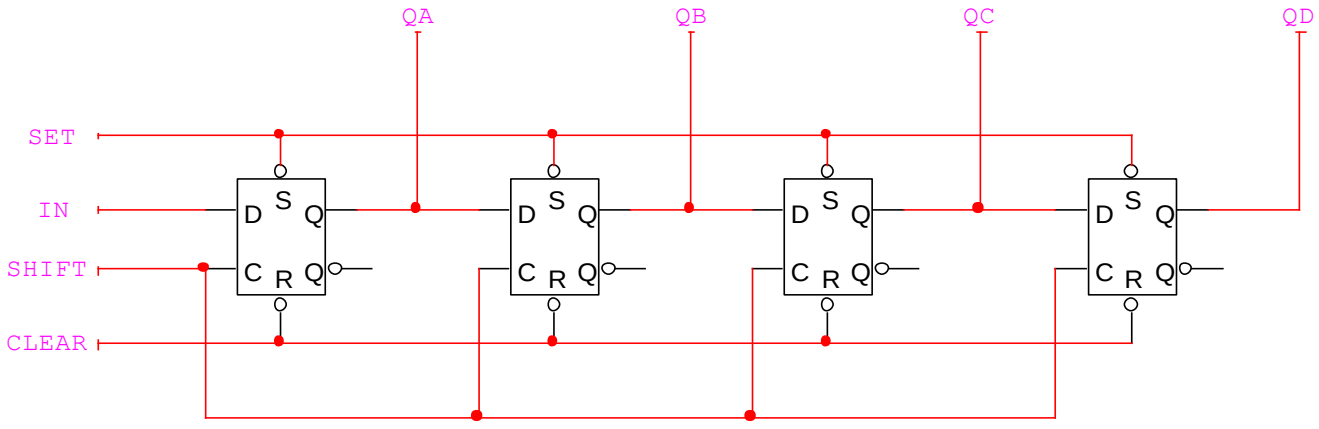
Note -- ↑ designates a clock pulse, *d* a don't care, *Q* the present state, and *Q** the next state.

Part 2 – Implement a Basic Shift Register on the IDL 800 Using D Flip-flops (SN7474).

a. Construct the 4-bit, serial-in, serial/parallel-out shift register shown below. Connect the various circuit I/O pins to the IDL-800 switches/LEDs as follows. Don't forget to also connect power (+5V) and ground.

IN – SW7 *SHIFT* – PULSE SWITCH A *SET* – SW1 *CLEAR* – SW0

QA – LED7 *QB* – LED 6 *QC* – LED 5 *QD* – LED4



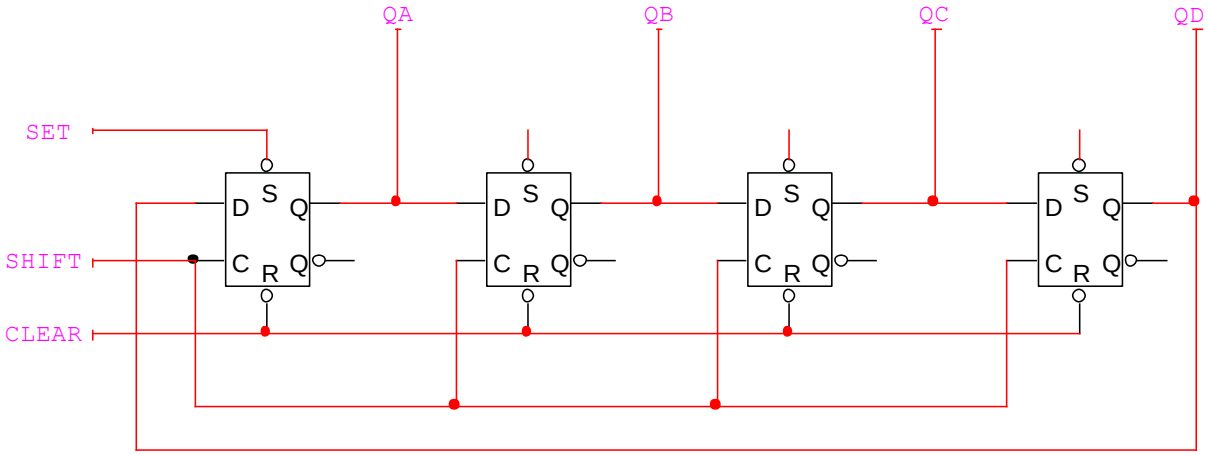
Part 2 (continued)

b. Experimentally analyze the behavior of the circuit as follows.

i. Place the *SET* and *CLEAR* inputs to logic 1
ii. Turn on the power
iii. Observe and record the values of the circuit outputs (*QA*, *QB*, *QC*, and *QD*)
iv. Place *SET* to logic 0 and *CLEAR* to logic 1
v. Observe and record the values of the circuit outputs (*QA*, *QB*, *QC*, and *QD*)
vi. Place *SET* to logic 1 and *CLEAR* to logic 0
vii. Observe and record the values of the circuit outputs (*QA*, *QB*, *QC*, and *QD*)
viii. Place the *SET* and *CLEAR* inputs to logic 1
ix. Place *IN* to logic 1
x. Enter four consequetive SHIFT pulses, observing and recording the outputs after each pulse
xi. Place *IN* to logic 0
xii. Enter four consequetive SHIFT pulses, observing and recording the outputs after each pulse

Part 3 – Implement a Four-Bit Ring Counter on the IDL-800.

a. Modify the basic register from Part 2 to realize the 4-bit ring counter shown below.

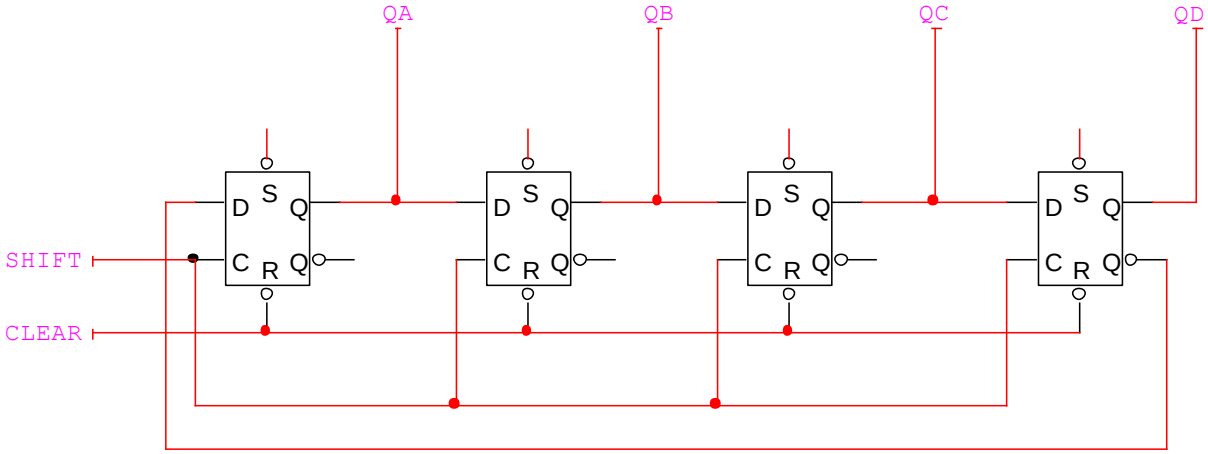


b. Use the *CLEAR* and *SET* inputs to place the counter in state 1000.
c. Enter four consecutive *SHIFT* pulses. Observe and record the state after each pulse.
d. Using the results from c, draw the state diagram of the ring counter.

e. How many states would be in a 6-bit ring counter? *N*-bit?

Part 4 – Implement a Four-Bit Twisted Ring Counter on the IDL 800.

a. Modify the ring counter to realize a 4-bit twisted-ring (Johnson) counter as shown below.



b. Connect the *SHIFT* input to the IDL-800 FUNCTION GENERATOR with amplitude at the Max setting. Place the FUNCTION GENERATOR in square-wave mode and the 1-HZ to 10-HZ frequency range. Place the freguency fine-tune knob in its minimum (CCW) position. These settings should produce a clock pulse with a frequency of about 1-HZ.
c. Place the shift-register in the all-0 state.
d. Observe and record the states of the counter in the form of a state diagram.

e. Slowly increase the frequency of the clock by turning the fine-tune knob clockwise. How does the state sequence change?

f. How many states would be in a 6-bit twisted-ring counter? *N*-bit?