The University of Texas at Arlington

Lecture 2

CSE 3442/5442

Embedded Systems I

Based heavily on slides by Dr. Roger Walker

Overview of PIC18 Family

- Class Only web site:
- http://crystal.uta.edu/~zaruba/CSE3442
- 1989, Microchip Technology introduced 8-bit microcontroller called PIC (Peripheral Interface Controller) – see web site at www.Microchip.com
- PIC18F452 Data sheets
- http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en010296
- PIC18F458
- http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en010301

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Lab Module and Online Book

- **Book that describes the PIC module used in the lab and other information on the PIC18: link on the class website.**
- **Kit used in lab: QwikFlash Development Kit No. 3 (Expanded Kit with QwikBreadboard 400 and Stand)** http://www.microdesignsinc.com/qwikflash/index.htm

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8-bit Microchip Families

- Microchip is currently the number one supplier of 8-bit microcontrollers.
- PIC families include 10xxx, 12xxx,14xxx, 16xxx, 17xxx, and 18xxx.
- PIC families are not upward compatible. All 8-bit processors.
- 12xxx/16xxx have 12-bit & 14-bit instructions
- PIC18xxx have 16-bit instructions

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PIC18 family

- PIC18 one of the higher performers of the Microchip's PIC families. There is now both a 32 bit PIC32 family and DSPIC (16 bit) with high performance.
- PIC families come in 18-to 80 pin packages.
- Select family based on performance, footprint, etc., needed, use selection guide: http://www.microchip.com/stellent/idcplg?IdcService=SS_GET_PAGE&nodeId=2661

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PIC18 features

- RISC architecture
- On-chip program ROM, data RAM, data EEPROM, timers, ADC,USART, and I/O Ports
- ROM, data RAM, data EEPROM, and I/O ports sizes varies within PIC18 family

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Figure 1-2. Simplified View of a PIC Microcontroller

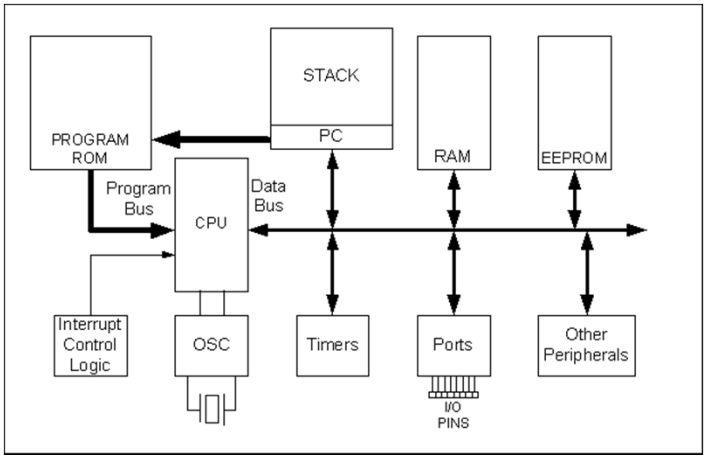

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Figure 1-3. PIC18 Block Diagram

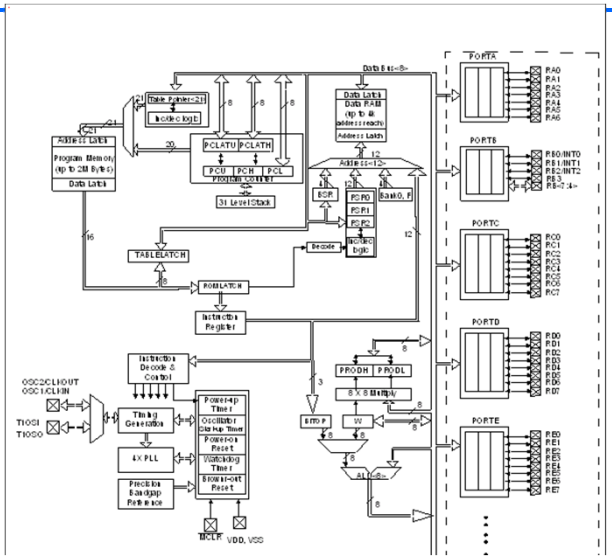

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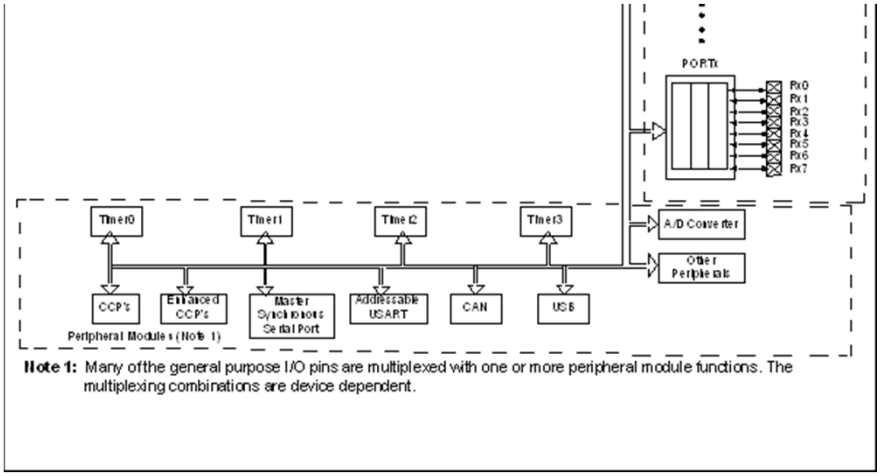
Figure 1-3. PIC18 Block Diagram (continued)



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PIC RAM/ROM Components

- ROM – program or code ROM (PIC18 can have up to 2 megabytes (2M) of ROM
- UV-EPROM for program memory– must have UV-EPROM eraser/programmer (burner ~20 minutes to erase)
- Flash memory PIC18F458 use for program development (EEPROM – electrically erasable PROM) – use PICkit 2 (from Microchip) using USB and PC.

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PIC Components cont.

- OTP version of PIC – one time programmable (ROM) versions available from Microchip (PIC16C452) – use for final production version – programmed at Microchip
- Masked versions of PIC – Provides a means of chip fabrication with program built in – minimum order but cost per IC cheapest of all methods.

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PIC Components cont.

- I/O Pins – 16 to 72 pins dedicated for I/O. PIC18 has 18 to 80.
- PIC18F8772 72 pins available for I/O.
- Other 8-bit microcontrollers besides the PIC, 8051 (Intel), 68HC11 (Motorola), Z8 (Zilog).

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Chapter 2 PIC Architecture & Assembly Language Programming

- WREG – 8 bit register in PIC (Working Register) – used the most

MOVLW K

Move (“MOV”) the number (“L” for “literal”) K (example 0xA), or 10 in decimal) - into the working register (“W”).

That is, load W with the value 0xA

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Moving to WREG

- MOVLW K ; move literal value K into WREG
- Once again K is an 8 value 0-255 decimal or 00-FF in hex
- Eg.
- MOVLW 25H ; move 25H into WREG (WREG = 25H)

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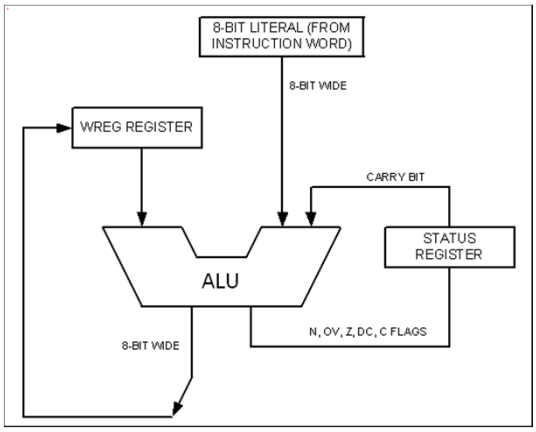
Figure 2-1. PIC WREG and ALU Using Literal Value



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Move and Add Instructions

- MOVLW 12H ;load value 12H -> WREG
- ADDLW 16H ;add 16H to WREG
- ADDLW 11H ;add 11H to WREG
- ADDLW 43H ;add 43H to WREG

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FILE REGISTER

- File Register – (data RAM) read/write memory used by CPU (varies from 32 bytes to .. depending on chip size (family)
- Divided into two sections
  - Special Purpose Registers (SFR)
  - General Purpose Registers (GPR) or (GP RAM)

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FILE REGISTER cont.

- SFR – specific functions –
  - ALU status
  - Timers
  - Serial communications
  - I/O Ports
  - A/D

  Example: the more timers the more SFR in a PIC

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FILE REGISTER – cont.

- GPR – The general-purpose registers – RAM locations used for data storage and scratch pad (8-bit) (data RAM size same as GFR size)

GPR varies between families, see Table 2-1, pp 44

Example:

PIC12F508 32bytes SFR – 7 bytes, GPR – 25 bytes

PIC 18F452 1792 bytes SFR – 256, GPR - 1536

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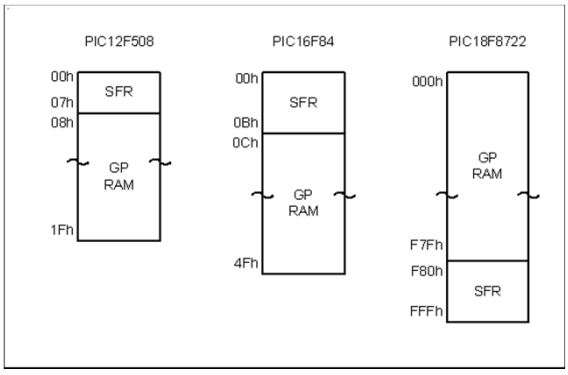
Figure 2-2. File Registers of PIC12, PIC16, and PIC18



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File Registers, cont.

- Access bank in the **PIC18**
- PIC File Register has a max of 4K or:

  000-FFFH

  Divided into 16 banks of 256 bytes. All PIC's have at least one bank – the access bank. The access bank divided into 2 sections of 128 bytes, SFR and GPR

00H – 7FH GPR, F80H – FFFH SFR (accessed directly

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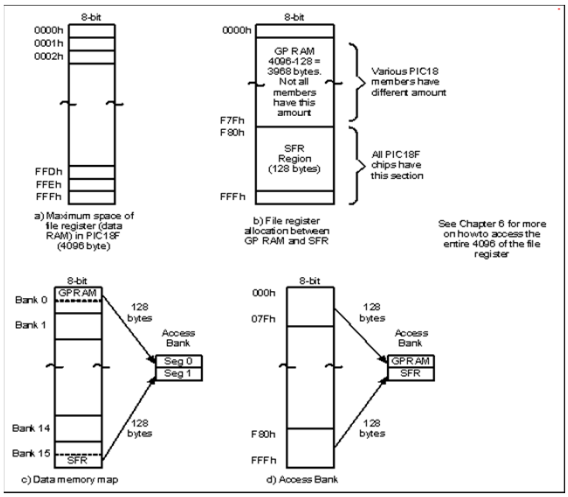
Figure 2-3. File Register for PIC18 Family



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Special Function Registers of the PIC18 Family.

F80h	PORTA	FA0h	PIE2	FC0h	----	FE0h	BSR
F81h	PORTB	FA1h	PIR2	FC1h	ADCON1	FE1h	FSR1L
F82h	PORTC	FA2h	IPR2	FC2h	ADCON0	FE2h	FSR1H
F83h	PORTD	FA3h	----	FC3h	ADRESL	FE3h	PLUSW1 *
F84h	PORTE	FA4h	----	FC4h	ADRESH	FE4h	PREINC1 *
F85h	----	FA5h	----	FC5h	SSPCON2	FE5h	POSTDEC1 *
F86h	----	FA6h	----	FC6h	SSPCON1	FE6h	POSTINC1 *
F87h	----	FA7h	----	FC7h	SSPSTAT	FE7h	INDF1 *
F88h	----	FA8h	----	FC8h	SSPADD	FE8h	WREG
F89h	LATA	FA9h	----	FC9h	SSPBUF	FE9h	FSR0L
F8Ah	LATB	FAAh	----	FCAh	T2CON	FEAh	FSR0H
F8Bh	LATC	FABh	RCSTA	FCBh	PR2	FEBh	PLUSW0 *
F8Ch	LATD	FACh	TXSTA	FCCh	TMR2	FECh	PREINC0 *
F8Dh	LATE	FADh	TXREG	FCDh	T1CON	FEDh	POSTDEC0 *
F8Eh	----	FAEh	RCREG	FCEh	TMR1L	FEEh	POSTINC0 *
F8Fh	----	FAFh	SPBRG	FCFh	TMR1H	FEFh	INDF0 *
F90h	----	FB0h	----	FD0h	RCON	FF0h	INTCON3
F91h	----	FB1h	T3CON	FD1h	WDTCON	FF1h	INTCON2
F92h	TRISA	FB2h	TMR3L	FD2h	LVDCON	FF2h	INTCON
F93h	TRISB	FB3h	TMR3H	FD3h	OSCCON	FF3h	PRODL
F94h	TRISC	FB4h	----	FD4h	----	FF4h	PRODH
F95h	TRISD	FB5h	----	FD5h	T0CON	FF5h	TABLAT
F96h	TRISE	FB6h	----	FD6h	TMR0L	FF6h	TBLPTRL
F97h	----	FB7h	----	FD7h	TMR0H	FF7h	TBLPTRH
F98h	----	FB8h	----	FD8h	STATUS	FF8h	TBLPTRU
F99h	----	FB9h	----	FD9h	FSR2L	FF9h	PCL
F9Ah	----	FBAh	CCP2CON	FDAh	FSR2H	FFAh	PCLATH
F9Bh	----	FBBh	CCPR2L	FDBh	PLUSW2 *	FFBh	PCLATU
F9Ch	----	FBCh	CCPR2H	FDCh	PREINC2 *	FFCh	STKPTR
F9Dh	PIE1	FBDh	CCP1CON	FDDh	POSTDEC2 *	FFDh	TOSL
F9Eh	PIR1	FBEh	CCPR1L	FDEh	POSTINC2 *	FFEh	TOSH
F9Fh	IPR1	FBFh	CCPR1H	FDFh	INDF2 *	FFFh	TOSU

* - These are not physical registers.

Figure 2-4.

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PIC18 File Register and Access Bank

- Bank switching required (as only 256 bytes are addressable) in File Registers if using more than 256 bytes:
- MOV***W*****F** used to copy from work register into file register:
  - MOVLW 12H ; 12H -> WREG
  - MOVWF 16H ; (WREG) -> File Register 16H

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WREG and Access Bank Instructions

- ADDWF fileReg, D

  Contents of WREG added to contents of fileReg. If D = 0, result placed in WREG

  If D = 1, result placed in fileReg

  e.g., **ADDWF 16H, 0** ; add the value contained in F-16H to the value of W (thus store in W).

  e.g., **ADDWF 16H, 1** ; add the value contained in W to the value of F-16H (thus store in F-16H)

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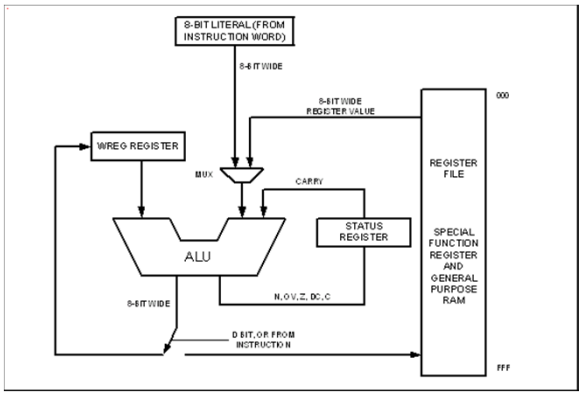
Figure 2-5. WREG, fileReg, and ALU in PIC18



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ALU Instructions WREG & fileReg (Table 2-2)

- ADDWF fileReg, d ;ADD WREG & fileReg
- ADDWFC fileReg, d ;ADD WREG & fileReg w/ Carry

.

.

- XORWF fileReg, d ;Exclusive-OR WREF w/ fileReg

See Table 2-3 (pp 53) for more Instructions using fileReg and WREG.

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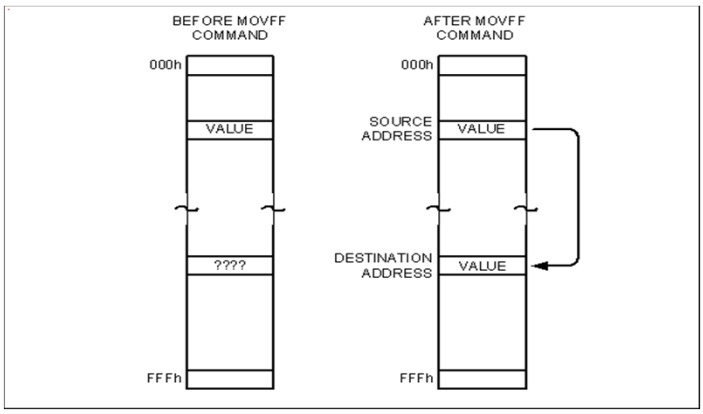
Figure 2-6. Moving Data Directly Among the fileReg Locations

MOVF FileRegS, FileRegD



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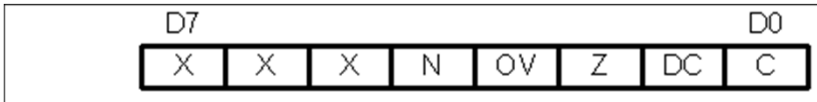
Bits of Status Register



C – Carry flag
DC – Digital Carry flag
Z – Zero flag
OV – Overflow flag
N – Negative flag
X – D5, D6, and D7 are not implemented, and reserved for future use.

Figure 2-7

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Flags Affected Following Execution of Most Instructions

- See Table 2-4. on page 60
- ADDLW can affect C, DC, Z, OV N
- ANDLW can affect Z
- MOVF can affect Z
- Move instructions (except for MOVF) will not affect any status bits

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ADDLW Example

- MOVLW 38H
- ADDLW 2FH

```
 38H        0011 1000
+2FH        0010 1111
 67H        0110 0111  WREG = 67H
```

C = 0 no carry out from bit 7
DC = 1 carry out from bit 3
Z = 0 WREG has value other than zero after addition

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ADDLW Example cont.

- MOVLW 9CH
- ADDLW 64H

```
 9CH        1001 1100
+64H        0110 0100
 100H       0000 0000  WREG = 00H
```

C = 1 carry out from bit 7
DC = 1 carry out from bit 3
Z = 1 WREG has value of zero after addition

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Flag Bits used in Branching

• BC	Branch if C = 1
• BNC	Branch if C ≠ 1
• BZ	Branch if Z = 1
• BNZ	Branch if Z ≠ 1
• BN	Branch if N = 1
• BNC	Branch if N ≠ 1
• BOV	Branch if OV = 1
• BNOV	Branch if OV ≠ 1

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Assignment for Next Class

- Finish Reading Chapter 0-2
- Download MPLAB X and C18
  - Link for MPLAB IDE
    can be found on class website.
  - Link for C18
    can be found on class website.

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