Objective: The term project consists of a design task that is based on knowledge you gained throughout the semester in the lecture and lab sessions. It is meant to challenge your ability to apply your understanding and knowledge of logical design to a practical problem. Appendix A describes the engineering design process that you are expected to follow in this project. This is an individual project, so group design and reporting is neither appropriate nor acceptable.

Grading: The project will be graded as follows and will count 15% toward your final CSE 2441 course grade. Failure to complete the project will result in a course grade of Incomplete.

60% -- design completed, simulated, implemented, tested and meets all specifications
15% -- project report completed and submitted and meets all requirements
15% -- design presentation delivered and submitted
10% -- additional features or enhancements above the required specifications

ABET outcome assessment: ABET, Inc. is the organization that accredits engineering programs in the United States and in many other countries around the world. One of the accreditation criteria requires documentation that students have demonstrated an ability to design a system, component, or process to meet desired needs within realistic constraints. The CSE 2441 term design project has been selected as one source of this documentation for the Computer Engineering Program at UT Arlington. Compliance with this requirement will be assessed using the rubric described in Appendix B. The assessment results will not affect your grade on the project.

Project timeline:

4/16/2013 -- Project assigned
4/16 – 5/3 -- Laboratory (127 ERB) will be open during regular lab hours for demonstration of your completed design and for consultation.
4/30 – 5/2 -- Project presentations made during class time, 2:00 to 3:20 PM.
5/3/2013 -- Last day to demonstrate project on the DE-1.
5/3/2013 -- Project report due by 9:00 PM.
**Project description:** Design a controller and display for a multiplier for multiplying two 4-bit unsigned binary numbers. The input/output signals for the multiplier are illustrated in the following block diagram and defined under design specifications.

![Block Diagram](image_url)

**Design Specifications:**

1. **Input/output definitions**
   a. $D$ and $R$ are the 4-bit unsigned binary numbers, multiplicand and multiplier, to be multiplied.
   b. $P$ is the 8-bit unsigned product of $D$ and $R$, i.e., $P = D \times R$.
   c. $Start$ is a control signal used in starting the multiply process.
   d. $Reset$ is a control signal used to restart process.
   e. $Done$ is a control signal that indicates when the multiplication operation is completed.
   f. $Clock$ is a control input that synchronizes the steps in the multiplication process.
   g. The left-most two seven segment displays should show the decimal value of $D$ until the multiplication is complete. The right-most two displays should similarly show $R$.
   h. The value of $P$ should be shown across all four displays once the multiplication operation is completed.

2. **Design a controller and display logic that meets the following criteria.**
   a. Satisfies the above I/O definitions.
   b. Uses the minimum number of flip flops.
   c. Uses the minimum number of combinational logic elements (gates, decoders, multiplexers, etc.).
   d. Does not produce any unwanted or undefined outputs.
   e. Incorporates the given arithmetic unit or an appropriate substitute or revision.

3. **Can be prototyped on an Altera DE-1 board.** Note that the seven-segment displays on the DE-1 are active-low (common anode) devices. The pushbutton switches on the DE-1 are high when not depressed and low when depressed.

4. **See Appendix C for more details about the multiplier design details.**
**Design and Implementation Tasks:**

1. Develop two alternative designs that meet the specifications. Select the design that best meets the specifications and other factors that you deem important. Explain the reasoning for your selection.
2. Capture your design of choice using Quartus II and verify that it meets specifications using Qsim.
3. Implement and test your design on an Altera DE-1 board.
4. Document your work in the laboratory notebook throughout the process.

**Deliverables:**

1. Hard copy and electronic copy of the Term Design Project Report. **Due by 9:00 PM on May 3 to carroll@uta.edu and shawn.geiser@mavs.uta.edu.** The report should be formatted as follows.
   - Cover sheet
   - Introduction
     - Overview of the project (including any added or special features)
     - Overview of the results
     - Unresolved problems and future plans
   - Final design description
     - Block diagram
     - Circuit schematic diagram from Quartus II
     - Pin-out assignments
     - Operating procedure
     - State diagram of the controller and display logic
   - Alternative design considerations
     - Alternatives considered
     - Reasons for selection of final design
   - Test Plan
     - Test strategy
     - Simulation results from Qsim
     - Test results from DE-1 implementation
   - Your self-assessment of the ABET outcome.

2. Hard copy of a seven to eight minute PowerPoint presentation (eight slides max) of your design and simulation results. **Must be presented in class on April 30 or May 2.**

3. Altera DE-1 implementation of the design. **Must be demonstrated in the laboratory on or before 5:00 PM on May 3.**

4. Your lab notebook.

   Note – you may pick up your report and notebook after course grades have been submitted. Unclaimed materials will be discarded after August 31, 2013.
Appendix A: Engineering Design Process

Specify the Problem

1. Identify and specifically define the problem with input from the customer
2. Research the need or problem
3. Identify criteria and constraints

Develop a Solution

4. Develop a list of possible solutions.
5. Explore possible solutions (cost/benefit, pros/cons)
6. Evaluate the options using criteria identified by the problem specification
7. Choose the optimum solution.

Implement a Prototype

8. Build a model or prototype

Evaluate the Prototype

9. Test and evaluate the solution

Refine and Complete the Design

10. Refine the design based on evaluation
11. Repeat Engineering Design Process with new design until acceptable solution for problem is completed.
12. Communicate the design to the customer.
Appendix B – ABET Assessment Rubric

“Student term project documentation” is the Term Project report plus the engineering lab notebook. In the assessment rubric point (EDP1 – EDP12) below, the 5, 3, and 1 levels indicate level of success in achieving the particular assessment point. The percentage given in braces after each rubric point indicates the percentage which that rubric point contributes to the overall assessment.

**Problem Specification - rubric points (total of 17%)**

EDP1: Student term project documentation includes Term Project description which contains the given problem to solve.  
Level 5: Term project description included  
Level 3: Term project description talked about but not included  
Level 1: Student documentation does not include problem description  
{2%}

EDP2: Student term project documentation shows evidence of research related to understanding the given problem.  
Level 5: Notes and references are recorded in the engineering notebook and/or properly cited references are used in the Term Project report  
Level 3: Notes are recorded without attribution in the engineering notebook and/or references are used in the Term Project report without proper citation  
Level 1: No evidence of research  
{5%}

EDP3: Student term project documentation identifies problem criteria and constraints  
Level 5: Criteria and constraints above and beyond those given in the Term Project description are documented and clearly identified in the engineering notebook and/or Term Project report  
Level 3: Criteria and constraints given in the Term Project description are clearly identified in the engineering notebook and/or Term Project report  
Level 1: Criteria and constraints are not addressed in term project documentation  
{10%}

**Solution Determination - rubric points (total of 30%)**

EDP4: Student term project documentation shows evidence of solution development  
Level 5: The engineering notebook and/or Term Project report document at least three approaches (or three places where multiple solutions are considered) to solving all or part of the Term project problem. Ex: Using counters or using primitive logic to implement part of the date mechanism would be two different approaches.  
Level 3: The engineering notebook and/or Term Project report document at least two choices for solving some part of the Term project problem.  
Level 1: The engineering notebook and/or Term Project report document that only one solution was ever considered OR no documentation exists.  
{18%}

EDP5: Student term project documentation shows consideration of each solution approach in terms of cost/benefit, pros/cons, risks/rewards or other analysis  
{5%}
Level 5: The engineering notebook and/or Term Project report document(s) meaningful analysis of each solution decision point.
Level 3: The engineering notebook and/or Term Project report document(s) meaningful analysis of at least two solution decision points.
Level 1: No analysis of solution decision points is documented.

EDP6: Student term project documentation shows evaluation of each solution approach in terms of the problem criteria and constraints {5%}

Level 5: The engineering notebook and/or Term Project report document(s) meaningful evaluation of each solution decision point.
Level 3: The engineering notebook and/or Term Project report document(s) meaningful evaluation of at least two solution decision points.
Level 1: No evaluation of solution decision points is documented.

EDP7: Student term project documentation shows choice of optimum solution approach in terms of the analysis and evaluation {5%}

5: The engineering notebook and/or Term Project report document(s) choices clearly with reasons and additional notations about tradeoffs or other issues.
3: The engineering notebook and/or Term Project report document(s) choices with some reasons recorded.
1: No choice rationale of solution is documented.

Implementation - rubric points {total of 10%}

EDP8: Student term project Quartus/Qsim design demonstrates model for solution {10%}

Level 5: The Quartus/Qsim design includes all required functionality
Level 3: The Quartus/Qsim design includes half of the required functionality
Level 1: The Quartus/Qsim design does not implement required functionality

Evaluation - rubric points {total of 15%}

EDP9: Student term project documentation shows testing and evaluation results for Quartus/Qsim design model of solution {15%}

Level 5: The engineering notebook and/or Term Project report describes tests that exercise all functions of the design done during implementation of Quartus/Qsim design and results
Level 3: The engineering notebook and/or Term Project report describes tests that exercise half of the functions of the design done during implementation of Quartus/Qsim design and results
Level 1: The engineering notebook and/or Term Project report has no description of tests done during implementation of Quartus/Qsim design and/or no results

Solution Refinement and Completion - rubric points {total of 28%}

EDP10: Student term project documentation shows changes made to Quartus/Qsim design model for solution based on results of testing and evaluation {10%}
Level 5: The engineering notebook and/or Term Project report document(s) all errors found and the corrections made to the implementation as a result of test evaluation during implementation of Quartus/Qsim design 
Level 3: The engineering notebook and/or Term Project report document(s) some of the errors found and the corrections made to the implementation as a result of test evaluation during implementation of Quartus/Qsim design

Level 1: The engineering notebook and/or Term Project report does not document(s) changes made as a result of test evaluation

EDP11: Student term project documentation and Quartus/Qsim design and DE-1 implementation provide a working and correct solution for the given problem {8%}

Level 5: The Quartus/Qsim design and DE-1 implementation successfully accomplishes all required functionality
Level 3: The Quartus/Qsim design and DE-1 implementation correctly accomplishes half of the required functionality
Level 1: The Quartus/Qsim design and DE-1 implementation accomplishes no correct functionality

EDP12: Student term project documentation and in-class presentation describes Quartus/Qsim design model for solution {10%}

Level 5: The Quartus/Qsim design is clearly and completely described
Level 3: Parts of the Quartus/Qsim design are described but not all or all is described but not clearly.
Level 1: The Quartus/Qsim design is not described.
Appendix C

Four by Four Unsigned Binary Multiplier Design Details

Top-Level Design

Arithmetic Logic
Controller Logic
Display Logic

Arithmetic Unit Datapath Design
Algorithmic State Machine (ASM) Description of the Multiplier

Start

\[ R(1) = 1? \]

\[ A \leftarrow A + D \]

Right Shift \( C:A:R \)

\[ CNT \leftarrow CNT + 1 \]

\[ C \leftarrow 0 \]

\[ CNT = 3? \]

End

Load (LD) Phase

Add (AD) Phase

Shift (ST) Phase

Hold (HD) Phase

Schematic Design of the Arithmetic Unit