

Lab 4 – LED Die Circuit

CSE 3323 – Electronics for Computer Engineering

In this lab, we will design together the high-level concepts required to build an LED Dice board (rolling a single die). Topics include Boolean logic, Karnaugh maps, 555-timers, counters, and proper LED driving. Then we will flesh out the low-level details regarding which specific components we will use.

Students work in pairs (except one group of 3) during lab time.

Each student will submit a PDF lab report (due by one week) regarding the lab measurements and the circuits built. Other required files are detailed on the last page.

What you specifically should include in your lab report is indicated in RED throughout this document. You should also elaborate to discuss the procedure of each individual circuit AND discuss your results/measurements/thoughts.

Lab reports are **individual work** but include your lab partner's name in your report.

Tools Used:

- **Digital Multimeters**
 - Thsinde 18B+ (yellow)
 - Mastech MS8268 (green)
- **Current-Limited Power Supplies**
 - DC Power Supply, Yihua YH-302D
 - DC Regulated Power Supply, Tekpower TP3005T
- **Digital Oscilloscope**
 - Siglent SDS 1202X-E, 200MHz
- **Wire cutters/strippers, probes, banana connectors, alligator clips, jumper wires, etc.**

Components Used:

Note: No components are listed in this document, instead they are organized in a separate **Bill of Materials** document on Blackboard named **"BOM_LED_Die.pdf"**

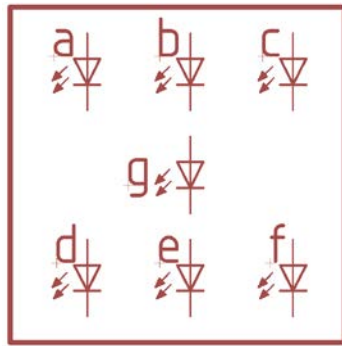
We will build two different versions of the LED Die Circuit:

- Version 1: Only uses NAND Gates and will be breadboarded in lab
- Version 2: Uses OR/AND/NAND Gates and will be a soldered PCB

Directed Part of Lab:

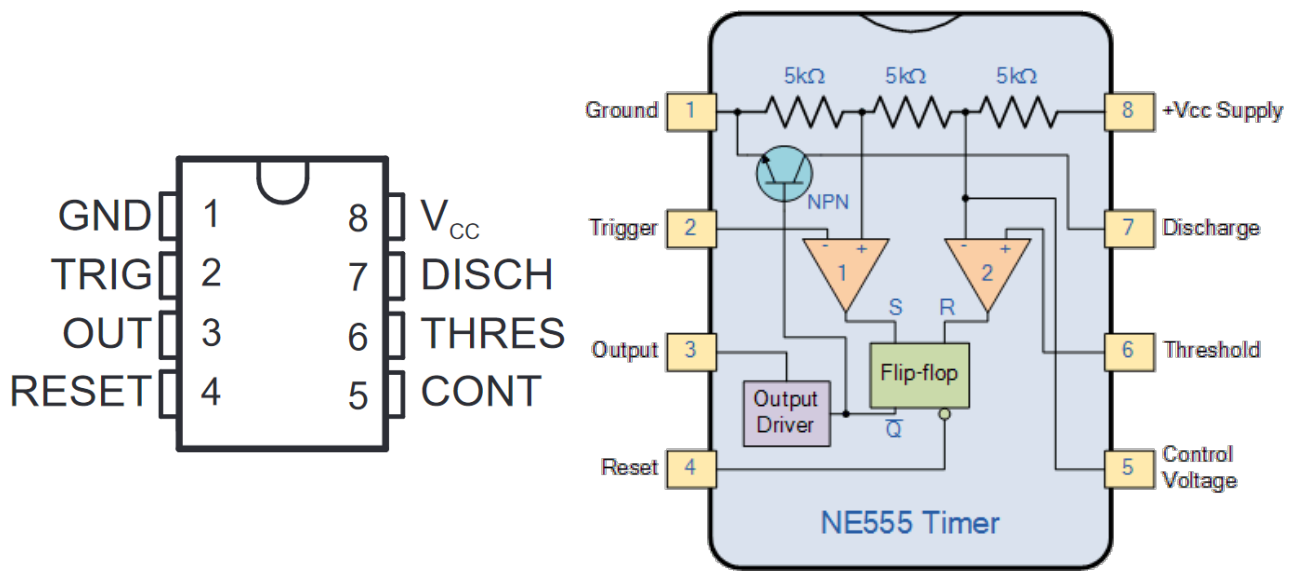
1. LED Die Circuit Requirements

- No programmable logic (i.e. no microcontrollers)
- User can toggle the power ON and OFF
- LEDs represent the die faces
- User presses a button and while the button is held down, the LEDs “roll” and cycle through all valid combinations
- When the user releases the button the LEDs stop cycling and “land” on a certain number/side of the die
- The user may at any time adjust the speed at which the LEDs cycle through the sequences (speed of the roll)
- It must not blow up or start a fire

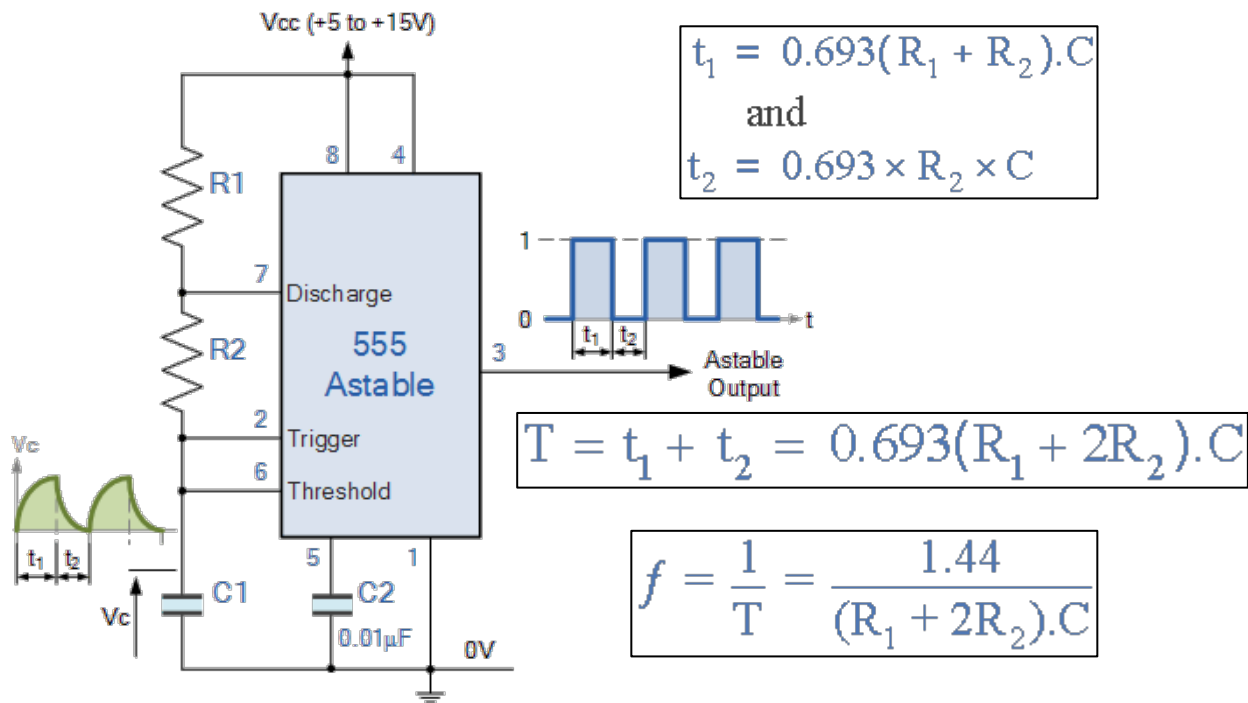


2. 555-Timer in Astable Mode

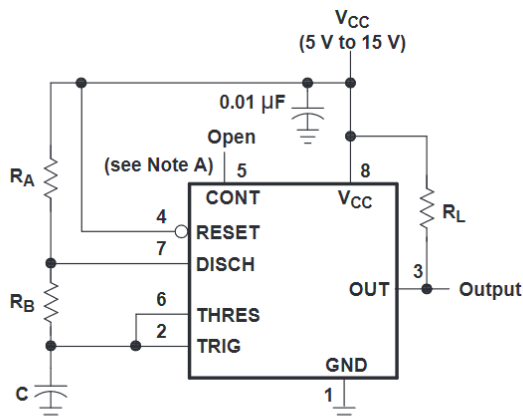
- We want a square wave clock signal whose frequency can be adjusted
- An output frequency range of ~1Hz to ~50Hz



From: https://www.electronics-tutorials.ws/waveforms/555_oscillator.html



From datasheet at: <https://www.mouser.com/ProductDetail/595-NE555P>



Pin numbers shown are for the D, JG, P, PS, and PW packages.
 NOTE A: Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.

Figure 12. Circuit for Astable Operation

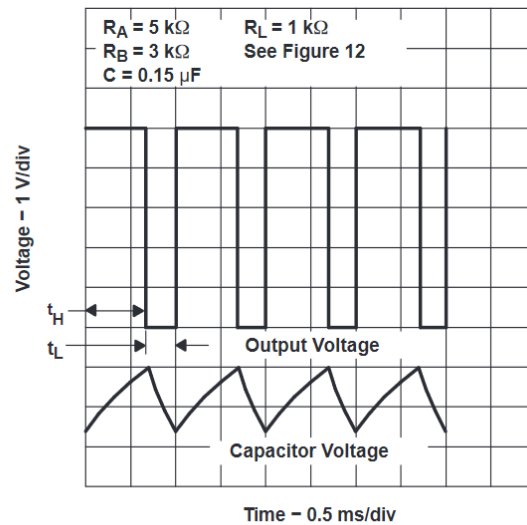


Figure 13. Typical Astable Waveforms

$$t_H = 0.693(R_A + R_B)C$$

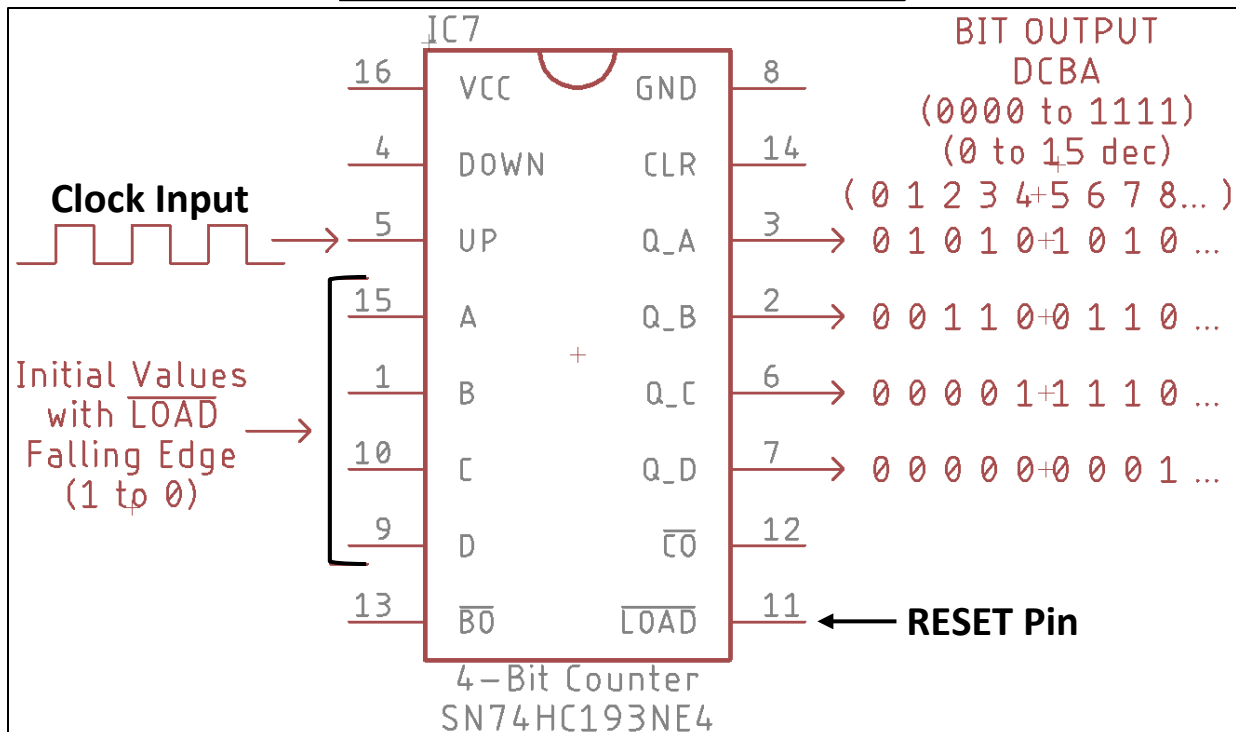
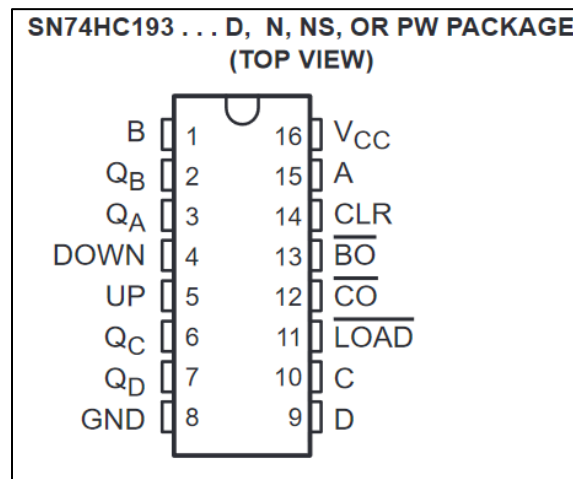
$$t_L = 0.693(R_B)C$$

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B)C}$$

$$\text{period} = t_H + t_L = 0.693(R_A + 2R_B)C$$

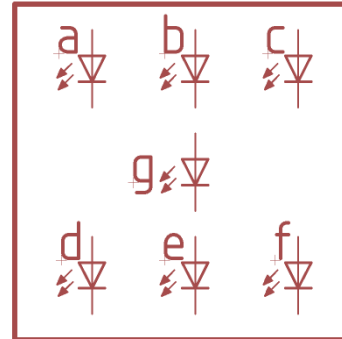
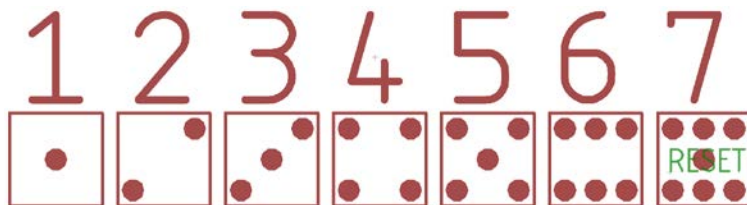
- c. For your lab report, work out the following Astable frequency calculations:
- With the requirements $C = 10\mu\text{F}$ and the desired **freq = 1Hz**, what are the values for R_A and R_B (also called R_1 and R_2)?
 - With the requirements $C = 10\mu\text{F}$ and the desired **freq = 50Hz**, what are the values for R_A and R_B (also called R_1 and R_2)?
 - Using the schematic “**LED Die v1**”, look at the Astable 555-timer portion of the schematic. Explain how it functions in your own words and using the component values listed in the schematic, calculate the **minimum** and **maximum** output frequencies when the potentiometer is completely turned CW or CCW.
 - Be sure to **SHOW ALL OF YOUR WORK** for all of these calculations

3. 4-Bit Counter IC



4. Karnaugh Maps

- How do we use K-Maps to map our **Counter Inputs** to our **LED Outputs**?
- For your lab report and your breadboarded circuit, derive all of the necessary K-Map tables for the Counter Inputs and LED Outputs below. Find the simplest **Final Logic** for this mapping.
- Be sure to **SHOW ALL OF YOUR WORK**



| Counter | | | | | | |
|---------|---|---|---|-----|------------------|----------------------|
| | C | B | A | | | |
| 1 | 0 | 0 | 1 | --> | g | Output To LEDs |
| 2 | 0 | 1 | 0 | --> | c, d | |
| 3 | 0 | 1 | 1 | --> | c, d, g | |
| 4 | 1 | 0 | 0 | --> | a, c, d, f | |
| 5 | 1 | 0 | 1 | --> | a, c, d, f, g | |
| 6 | 1 | 1 | 0 | --> | a, b, c, d, e, f | |
| 7 | 1 | 1 | 1 | --> | RESET Counter | |

| Final Logic | |
|-------------|----------------------------|
| ??? | = g |
| ??? | = a = f |
| ??? | = e = b |
| ??? | = c = d |
| ??? | = $\overline{\text{LOAD}}$ |

| | | |
|---|---|---|
| a | b | c |
| g | | |
| d | e | f |

C B A

| |
|---|
| g |
|---|

0 0 1

| | |
|---|---|
| | c |
| d | |

0 1 0

| | | |
|---|---|---|
| | g | c |
| d | | |

0 1 1

| | |
|---|---|
| a | c |
| d | f |

1 0 0

| | | |
|---|---|---|
| a | | c |
| d | g | f |

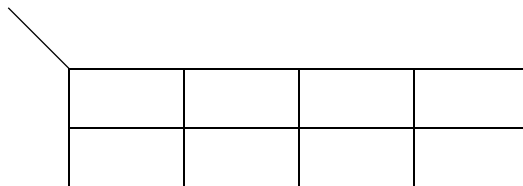
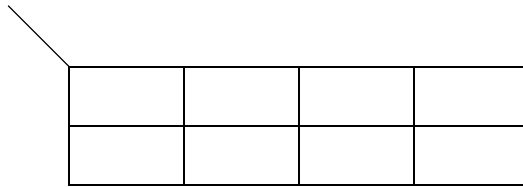
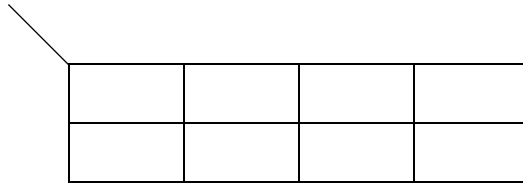
1 0 1

| | | |
|---|---|---|
| a | b | c |
| d | e | f |

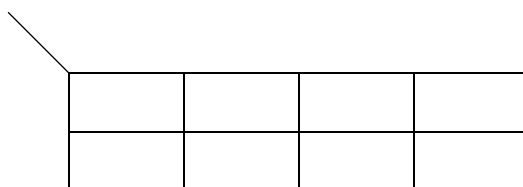
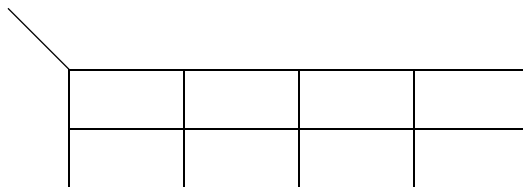
1 1 0

RESET

1 1 1

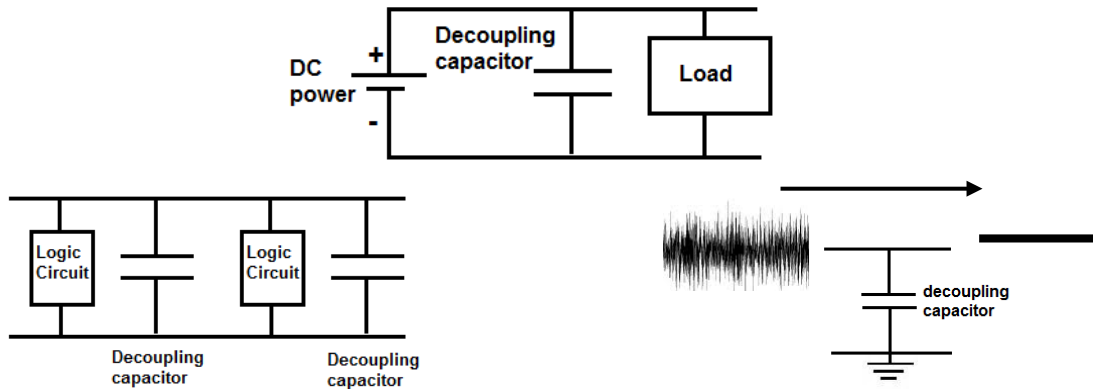


Final Logic
 = g
 = a = f
 = e = b
 = c = d
 = LOAD

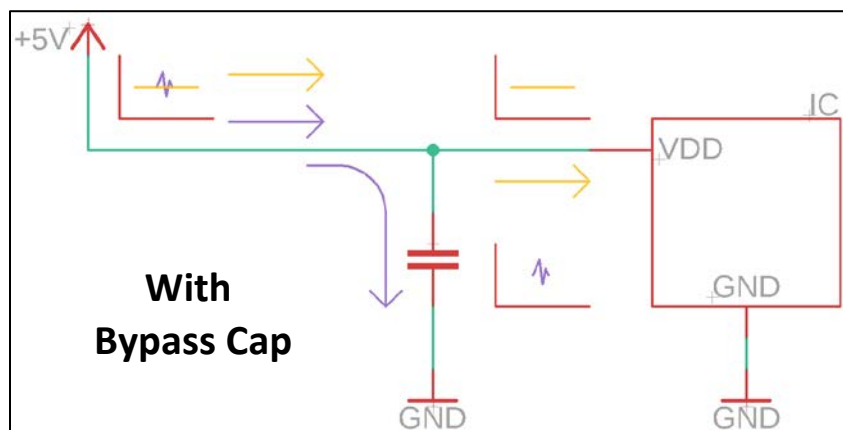


5. Bypass Capacitors (also called Decoupling Capacitors)

- These are used to decouple a portion of a circuit (like an IC's power input) from AC voltages, random voltage spikes, or noises caused by other circuit components. When placed near the VDD or VCC input of an IC, these capacitors can protect it from damage by immediately shunting or shorting the voltage spike directly to GROUND.
- "Pass unwanted AC to GND, DC is blocked and doesn't flow through CAP"
- [More Details 1](#), [More Details 2](#)



Remove noise, spikes, and "unwanted AC" seen by the IC's Power Pins



Individual Part of Lab:

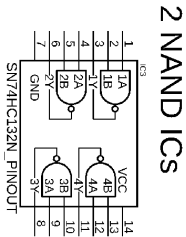
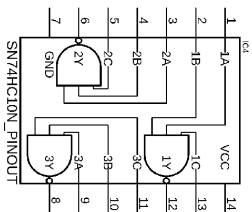
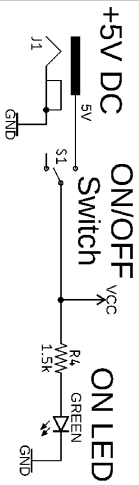
1. **Breadboard** (Work in Pairs)
 - a. Breadboard the circuit “**LED Die v1**”
 - b. All components are included in the schematic but there are 8 connections intentionally left disconnected. The logic between the Counter and the LEDs is also missing. You need to derive the proper K-Maps, find the final logic, and then translate that logic using only NAND gates.
 - c. Build the circuit in a modular fashion to simplify debugging:
 - i. Build power input/switch/green LED, then test...
 - ii. Build 555-Timer circuit, then test output square waveform...
 - iii. Build counter circuit, combine with 555, test each output...etc.
 - d. **Demo your working circuit when it is fully complete**

2. **PCB Soldering** (Individual Work, not pairs)
 - a. Solder the printed circuit board of the circuit “**LED Die v2**”
 - b. Take your time placing components and soldering, make it look professional
 - c. When you power it up for the 1st time, don't use the DC Barrel jack or the wall adapter. Instead use the +5V and GND clips on the PCB powered via the benchtop power supply; this way you can limit the current in case there is an accidental soldering short.

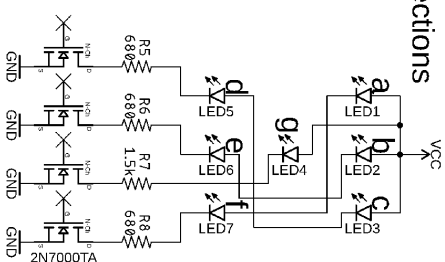
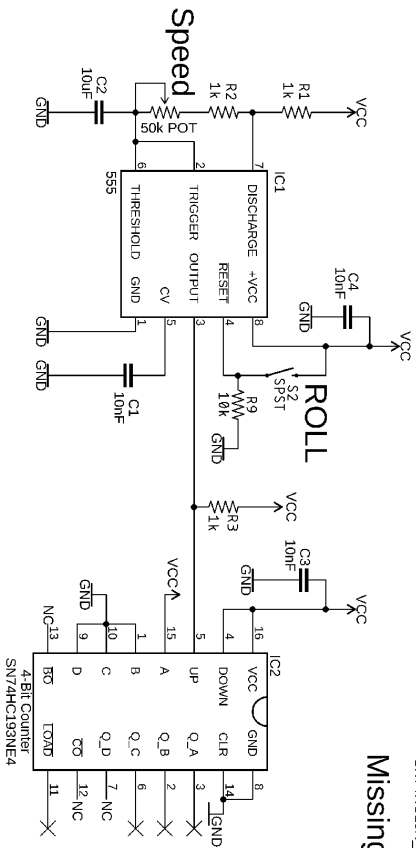
Additional Submission Details:

ZIP up all 3 of these files into a single zip file and upload to Blackboard

1. **Lab Report (.pdf)**
 - a. Include all of the details indicated above in **RED**
2. **Schematic File (.sch)**
 - a. Using EAGLE, draw your version of the full “**LED Die v1**” circuit. The wiring and connections need to be the same “electrically” but instead of copying EXACTLY from the image we provided, arrange components as you see fit and alter the arrangement of the pinouts of the ICs if you wish.
 - b. You will most likely have to create a few components yourself, so be sure to reference the datasheets for the non-standard components (Counter, Logic Gates, etc.). Package footprints (physical dimensions) need to be accurate.
 - c. The Bill of Materials document has all the datasheet links
 - d. Include part numbers and component values in the SCH diagram if applicable
3. **PCB File (.brd)**
 - a. Convert your .SCH file into a PCB
 - b. Arrange all the components in a logical and efficient manner
 - c. Keep the overall blueprint (size) of the board small and tight
 - d. You may use either single or double layer routing



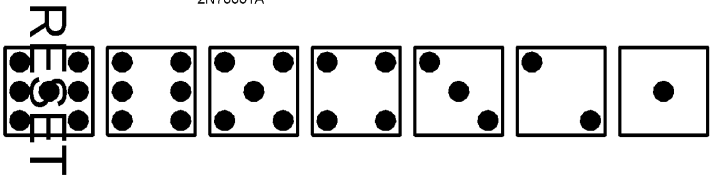
Missing Logic and Connections indicated by 8 X



| Astable Frequency Ranges | | | |
|--------------------------|----|--------|--------------|
| C | R1 | R2+POT | FreqOutput |
| 10uF | 1k | 1k | 48.00 Hz MAX |
| 10uF | 1k | 51k | 1.39 Hz MIN |

| Counter | | Output To LEDs | |
|---------|---|----------------|---|
| C | B | A | |
| 1 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 |
| 3 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 |
| 5 | 1 | 0 | 1 |
| 6 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 |

| Final Logic | |
|-------------|--|
| = g | |
| = a = f | |
| = e = b | |
| = c = d | |
| = LOAD | |



LED Die V1

UTA: CSE 3323 - Electronics

Breadboard Version with NANDS

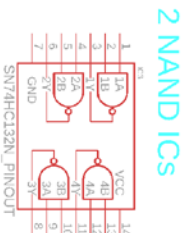
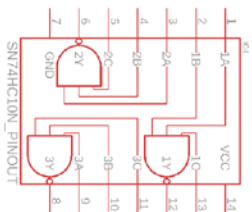
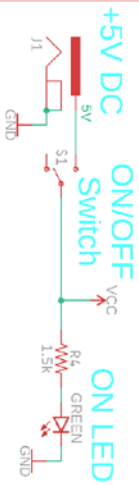
TITLE: LED_Die_V1_NEW

Document Number:

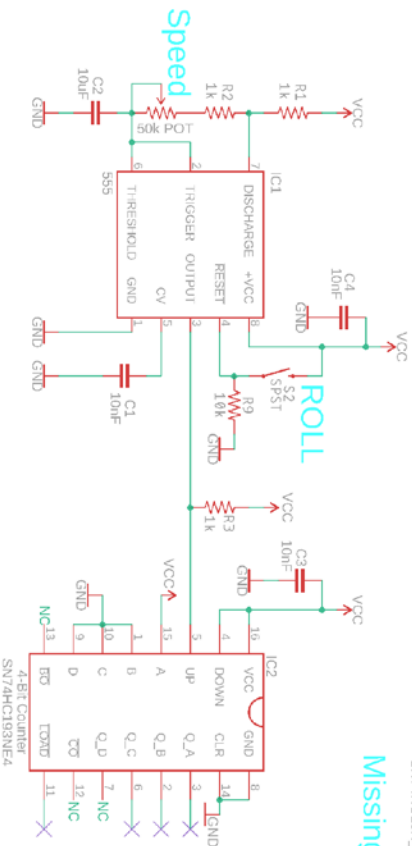
Date: 2/18/2019 11:00 PM

Sheet: 1/1

REV:



Missing Logic and Connections indicated by 8 X

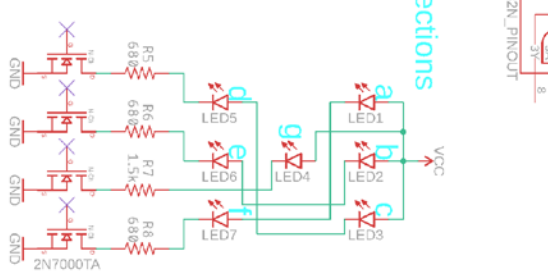


Astable Frequency Ranges

| C | R1 | R2+POT | FreqOutput |
|------|----|--------|--------------|
| 10uF | 1k | 1k | 48.00 Hz MAX |
| 10uF | 1k | 51k | 1.39 Hz MIN |

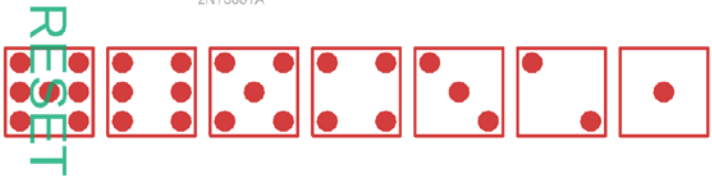
Counter

| Counter | CBA | Output To LEDs |
|---------|-----|------------------|
| 1 | 001 | g |
| 2 | 010 | c, d |
| 3 | 011 | c, d, g |
| 4 | 100 | c, d, g |
| 5 | 101 | a, c, d, f |
| 6 | 110 | a, c, d, f, g |
| 7 | 111 | a, b, c, d, e, f |



Final Logic

- = g
- = a = f
- = e = b
- = c = d
- = LOAD



LED Die V1

UTA: CSE 3323 - Electronics

Breadboard Version with NANDS

| | |
|--------------------------|------------|
| TITLE: LED_Die_v1_NEW | REV: |
| Document Number: | |
| Date: 2/18/2019 11:00 PM | Sheet: 1/1 |