Introduction to Sequential Logic Circuits
(Class 8.2 – 3/7/2013)

CSE 2441 – Introduction to Digital Logic

Spring 2013

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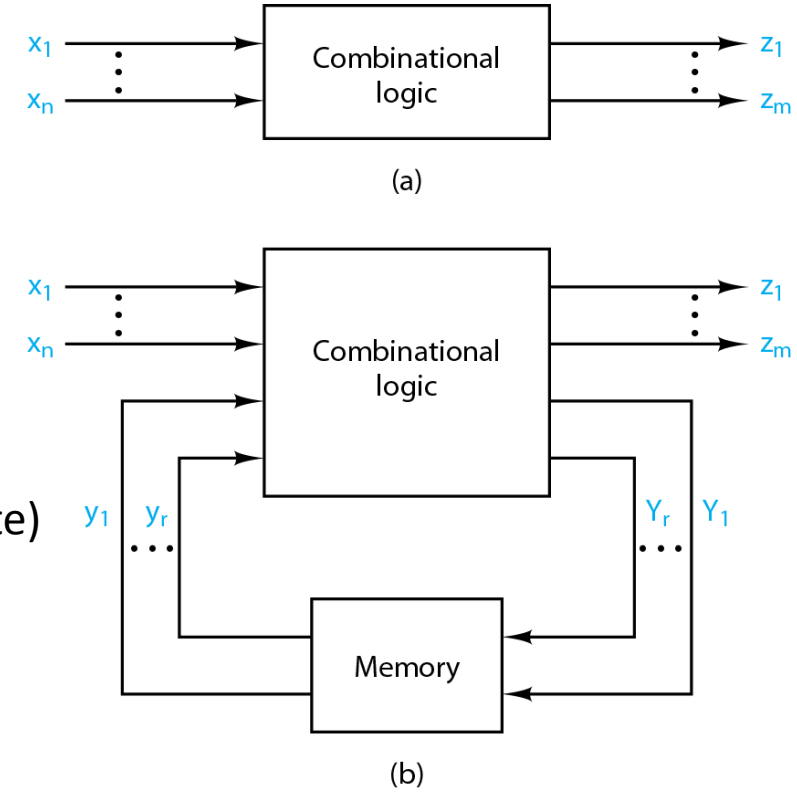
Today's Topics

- Sequential circuit models
  - Block diagram
  - State diagrams and state tables
  - Finite state machines (FSM)
- Types of sequential circuits
  - Synchronous (clocked)
  - Asynchronous
- Memory elements
  - Latches
  - Flip-flops
- Registers and shift registers
  - Generic devices
  - Standard 7400-series devices

The Sequential Circuit Model



$(x_1,\ldots,x_n)$ – Input

$(z_1,\ldots,z_m)$ – Output

$(y_1,\ldots,y_r)$ – Present State (state)

$(Y_1,\ldots,Y_r)$ – Next State

Figure 6.1

$$z_i = g(x_1,\ldots,x_n,y_1,\ldots,y_r) \text{ for } i = 1,\ldots,m$$

$$Yi = g(x_1,\ldots,x_n,y_1,\ldots,y_r) \text{ for } i = 1,\ldots,r$$

Types of Sequential Circuits

- Synchronous (clocked) circuits
- Asynchronous – will not cover in CSE 2441
  - Pulse mode
  - Fundamental mode

State Tables and State Diagrams (Synchronous Circuits)

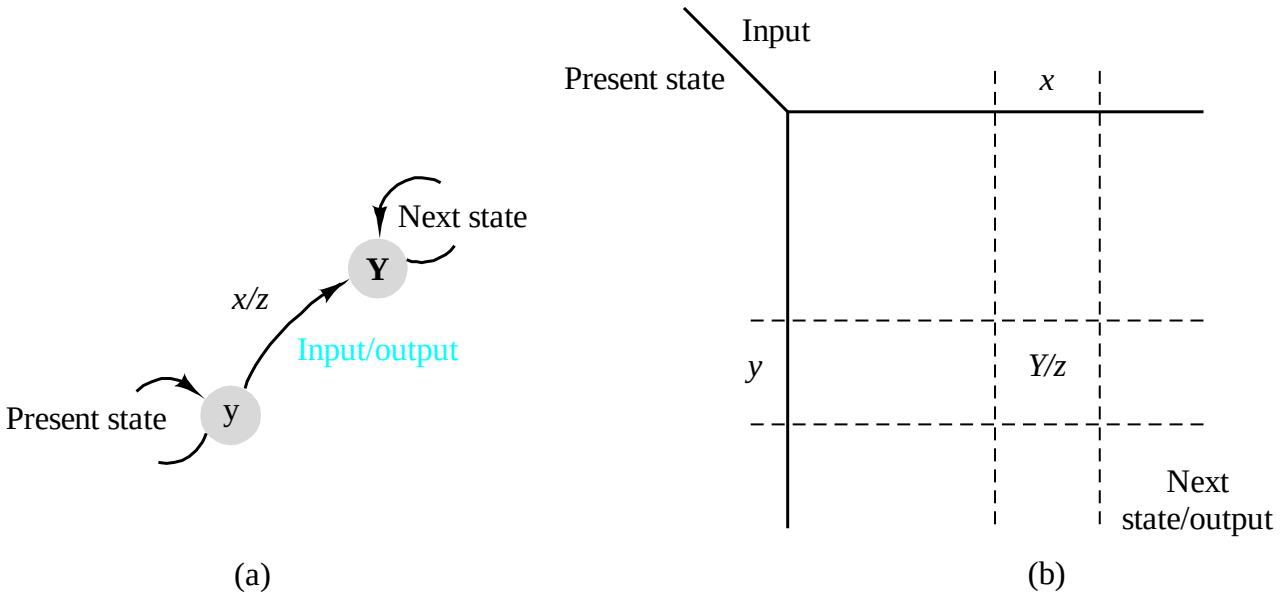
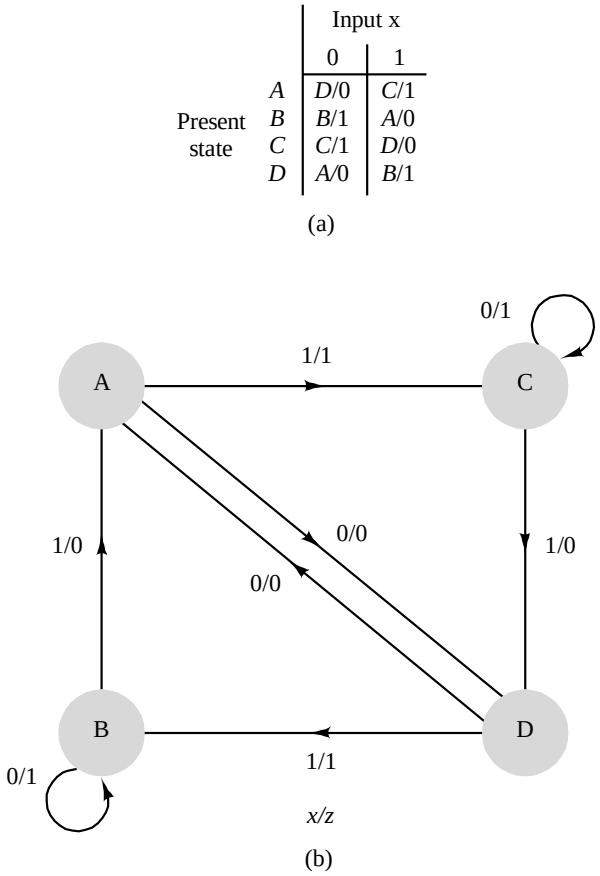


Figure 6.2

Sequential Circuit Example (Finite State Machine Model)



Present state	Input x = 0	Input x = 1
A	D/0	C/1
B	B/1	A/0
C	C/1	D/0
D	A/0	B/1

(a)

(b)

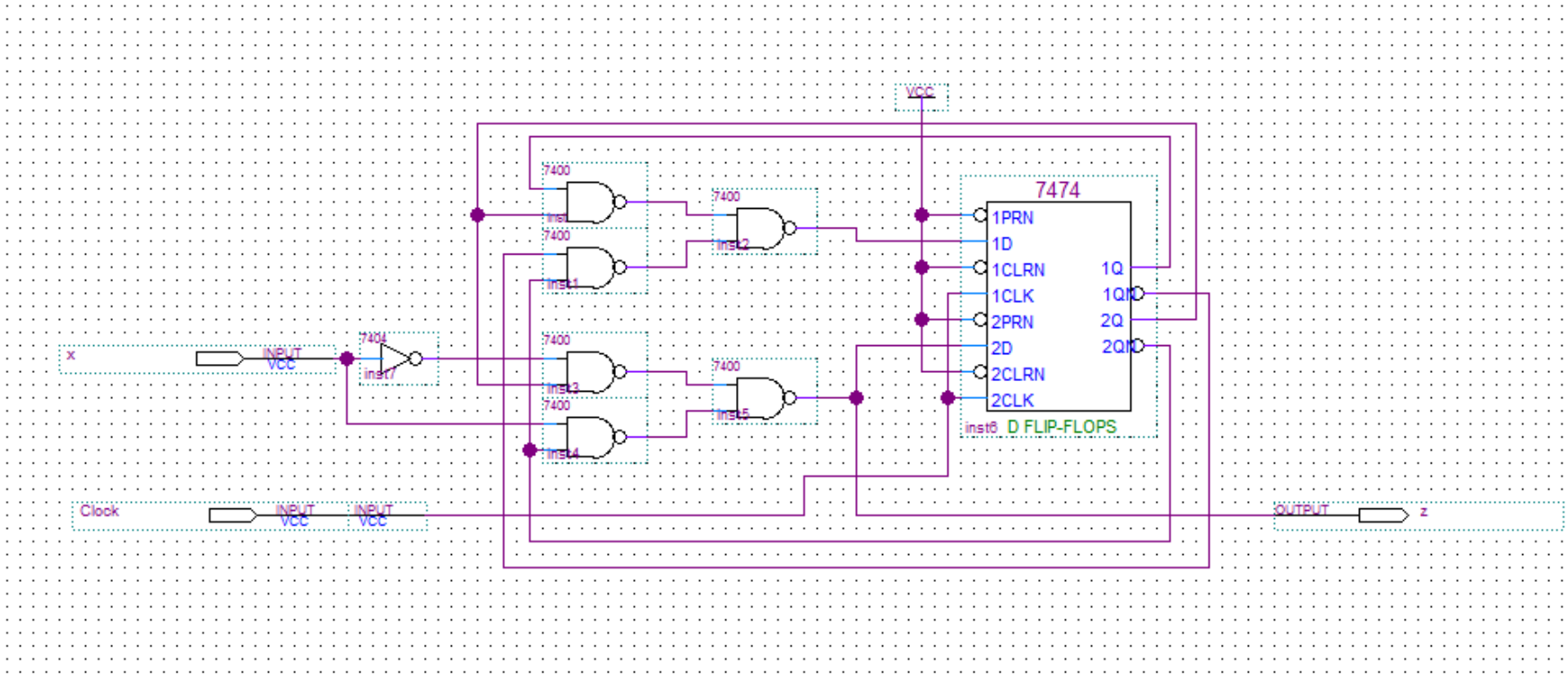
Figure 6.3

- Given
  - Input sequence
    x = 0110101100
  - Starting state *A*
- The machine behaves as follows

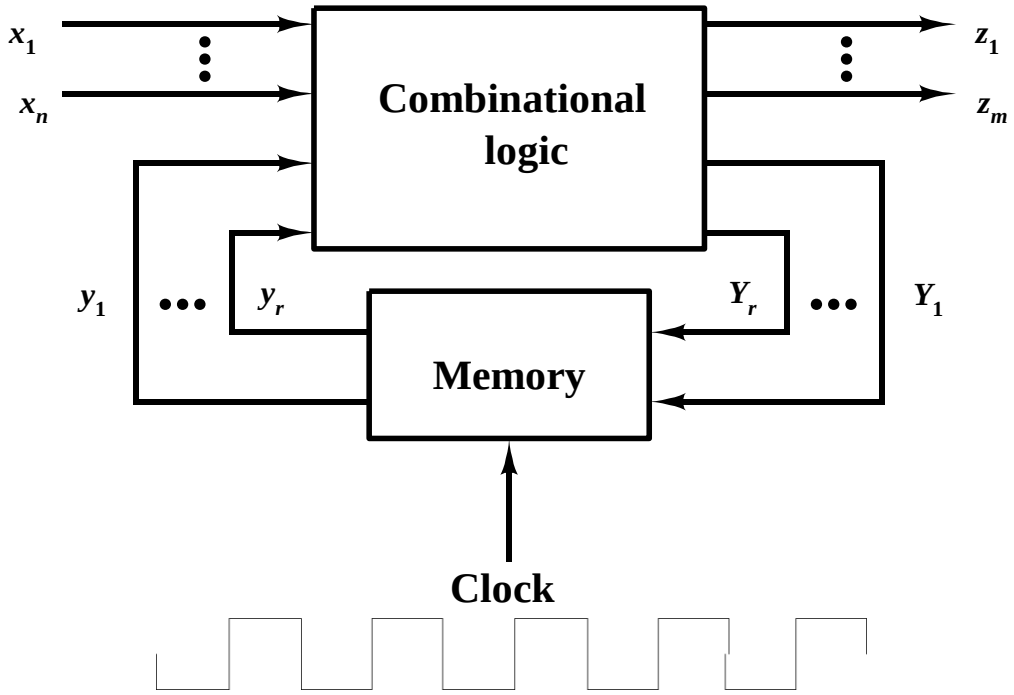
t	0	1	2	3	4	5	6	7	8	9	10
x	*0*	*1*	*1*	*0*	*1*	*0*	*1*	*1*	*0*	*0*	
y	*A*	*D*	*B*	*A*	*D*	*B*	*B*	*A*	*C*	*C*	*C*
Y	*D*	*B*	*A*	*D*	*B*	*B*	*A*	*C*	*C*	*C*	
z	*0*	*1*	*0*	*0*	*1*	*1*	*0*	*1*	*1*	*1*	

- Response
  - Output sequence
    z = 0100110111
  - Final state *C*

Realization Using D Flip-Flops



Synchronous Sequential Circuits



- State changes occur in synchronization with the clock signal
- Typical memory devices – D flip-flops, JK flip-flops

Types of Memory Elements

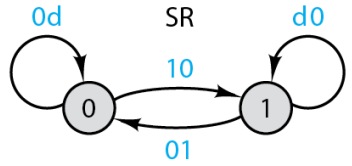
- Synchronous circuits
  - D flip-flop
  - JK flip-flop
  - SR flip-flop
  - T flip-flop
- Asynchronous circuits
  - Delay line (propagation delay)
  - SR latch
  - D latch

Set-Reset (SR) Latch

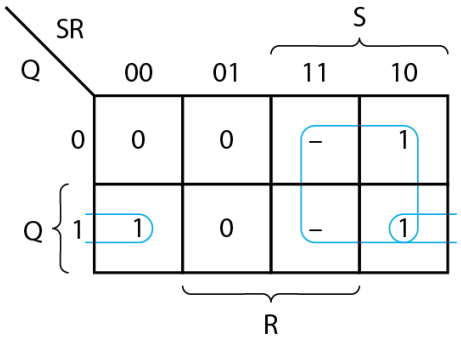
- Basic bistable, unclocked memory element
- Uses -- Memory in asynchronous circuits, component in clocked flip-flops

Excitation inputs S	R	Present state Q	Next state Q*	
0	0	0	0	No change
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	¥	Not allowed
1	1	1	¥	

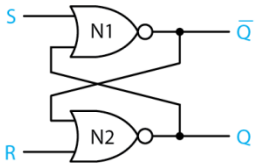
(a)

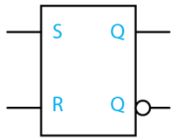


(b)



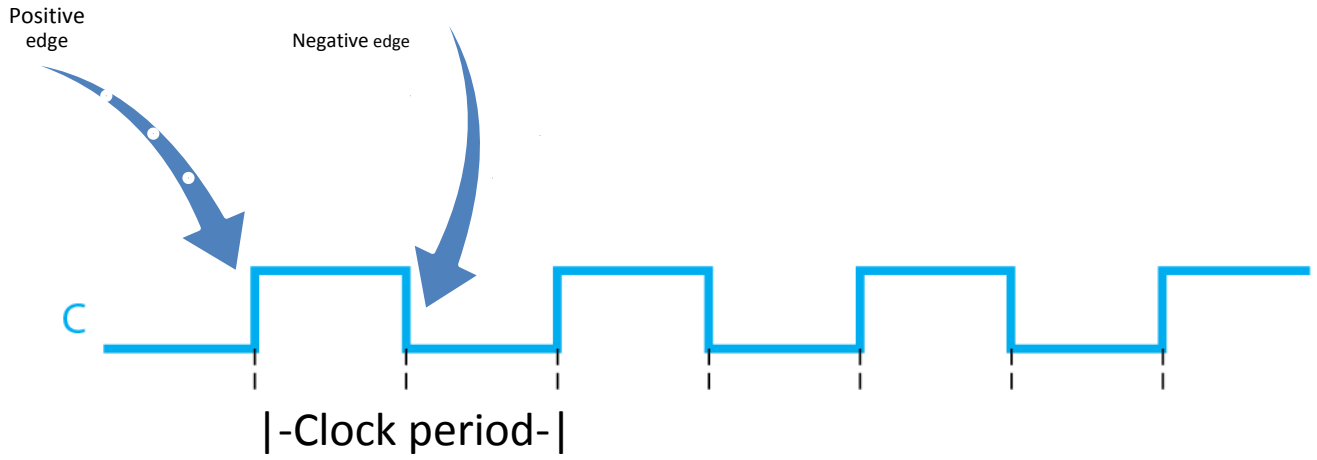
(c)





Characteristic Equation *Q* = S + R'Q*

Basic Clock Signal Terminology

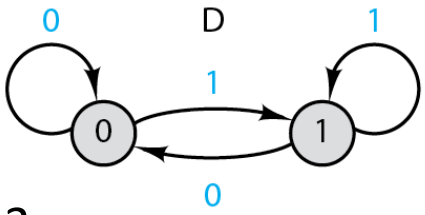


Positive edge – low to high transitions
Negative edge – high to low transitions
Clock period (t_c) – time between two positive edges.
Clock cycle – same as clock period.
Duty cycle -- % of cycle that is in a high state (50% in above case)
Clock frequency – $1/t_c$

SN7474 – Dual Positive Edge-Triggered D Flip-Flop

D	Q	C	Q*	
0	0	⎍	0	Store 0
0	1	⎍	0	
1	0	⎍	1	Store 1
1	1	⎍	1	

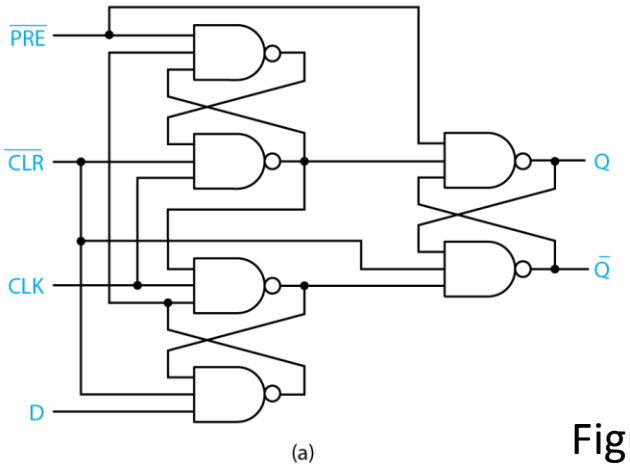
(a)



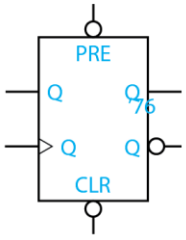
(b)

Figure 6.23

Characteristic equation – *Q* = D*



(a)



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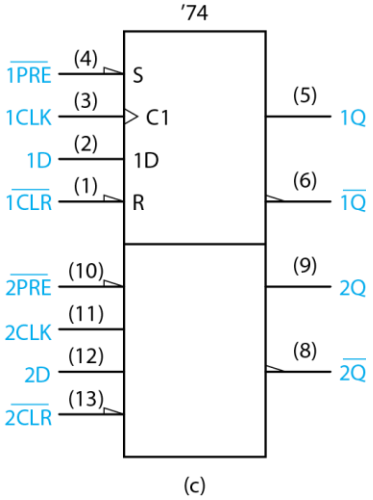


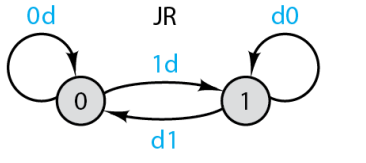
(c)

Figure 6.28

SN7476 – Dual Pulse-Triggered JK Flip-Flop

J	K	Q	C	Q*	
0	0	0	⎍	0	Hold
0	0	1	⎍	1	
0	1	0	⎍	0	Reset
0	1	1	⎍	0	
1	0	0	⎍	1	Set
1	0	1	⎍	1	
1	1	0	⎍	1	Toggle
1	1	1	⎍	0	

(a)



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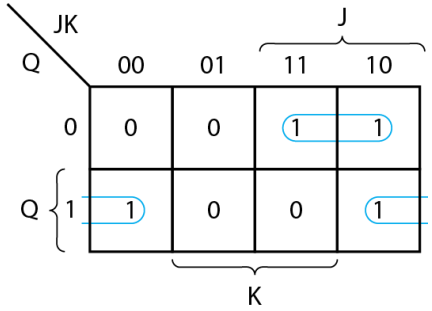
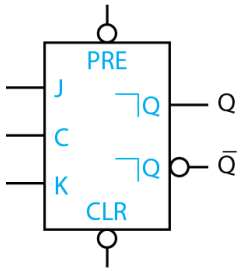
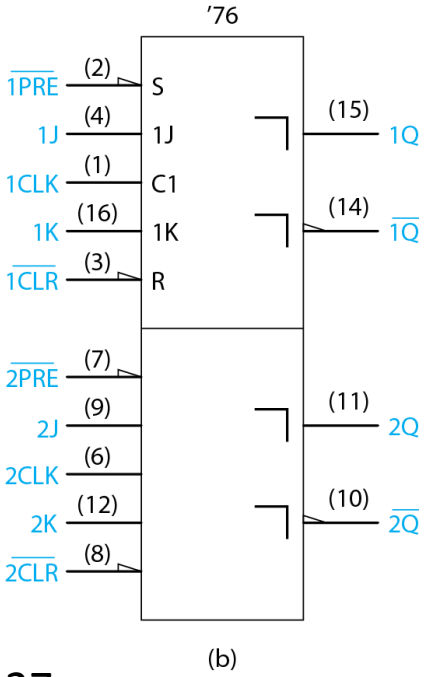


(c)

Figure 6.25



(a)

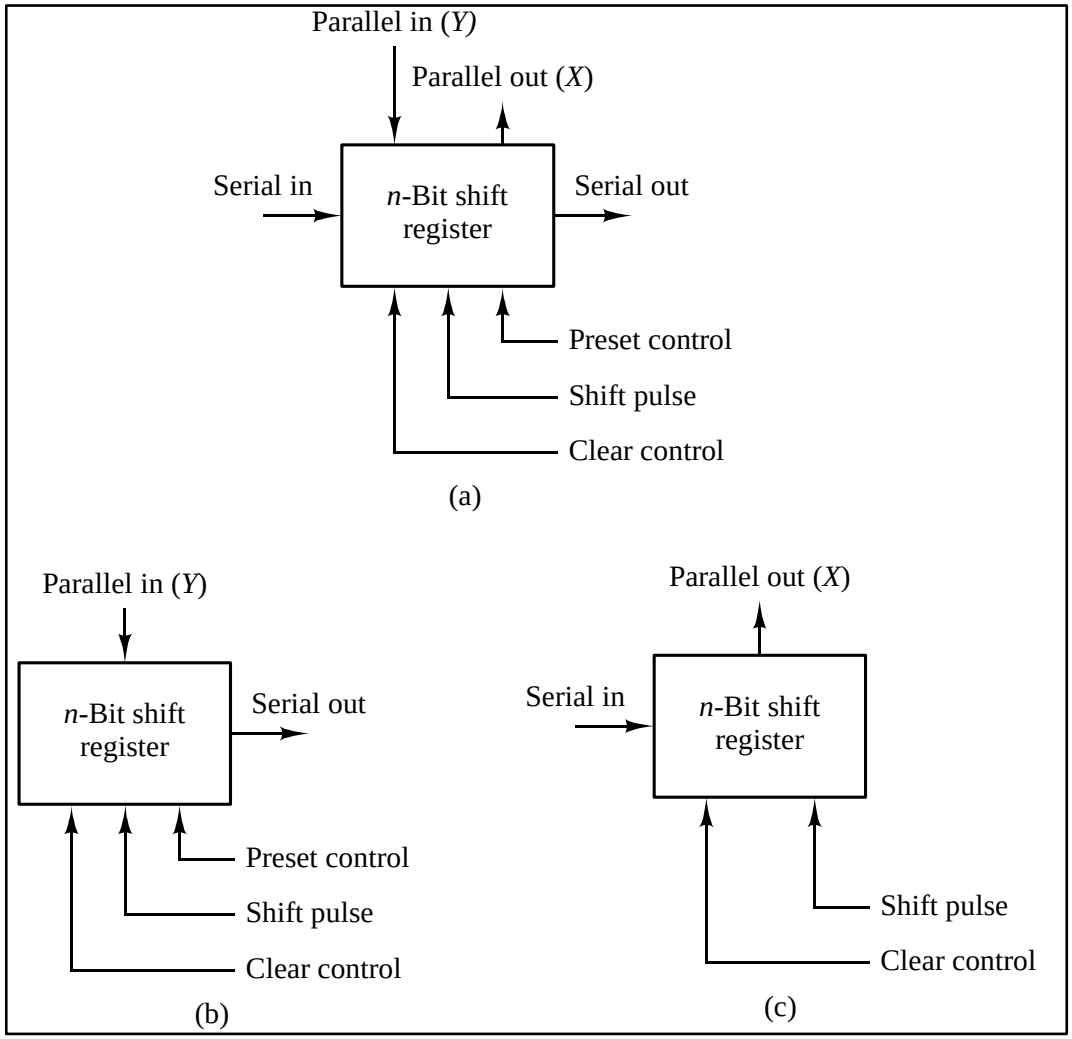


(b)

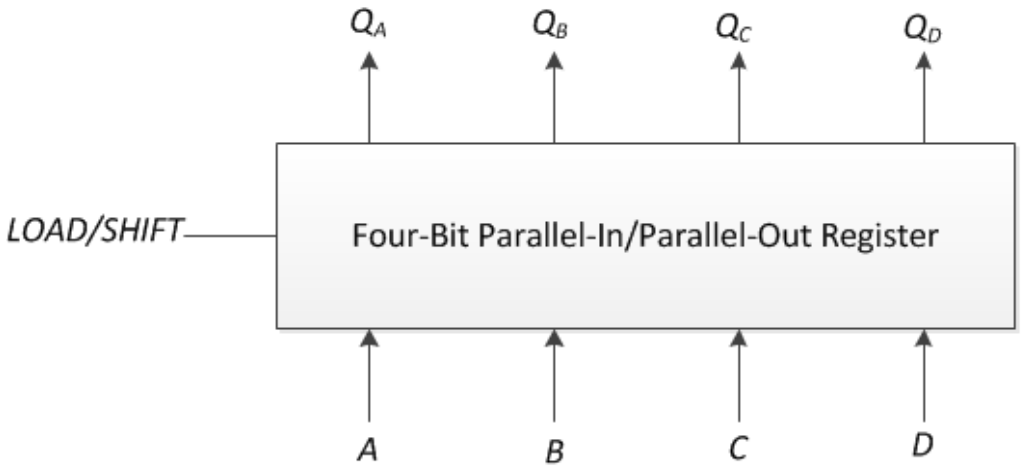
Figure 6.27

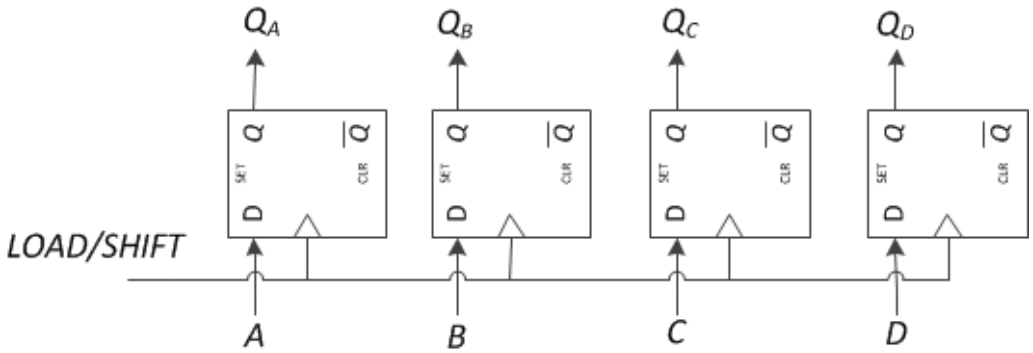
Characteristic equation *Q* = K'Q + JQ'*

Generic Shift Register

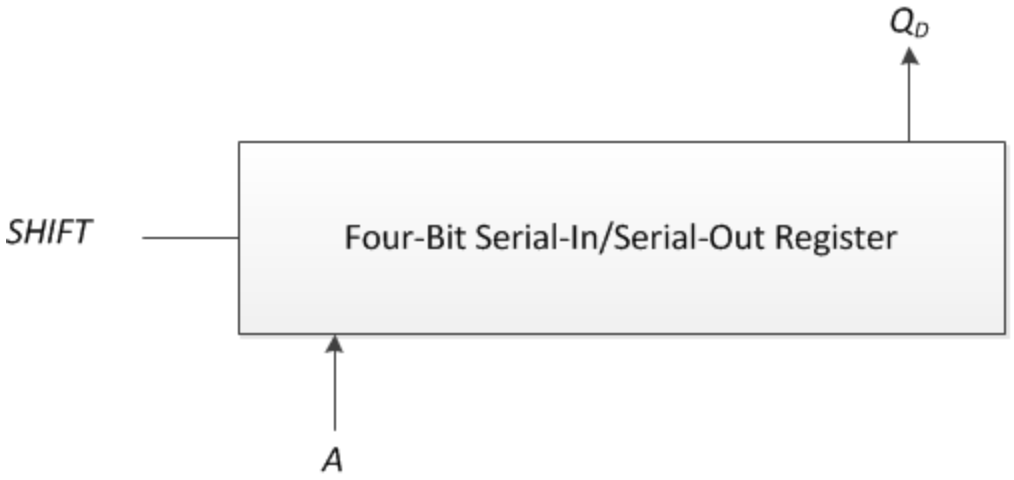


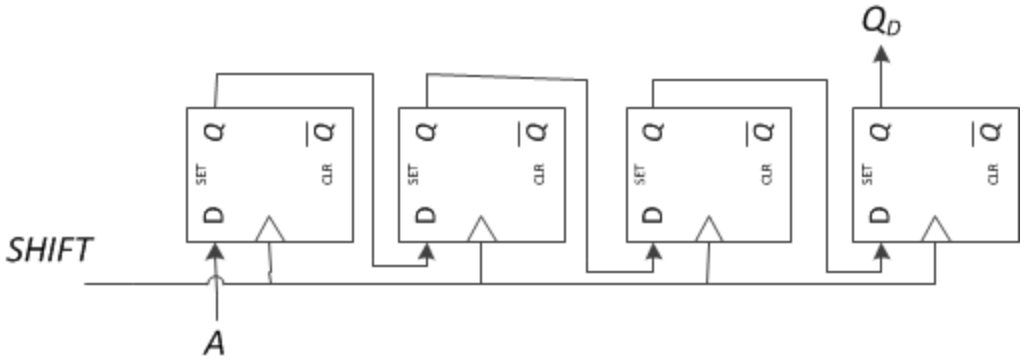
Basic Register



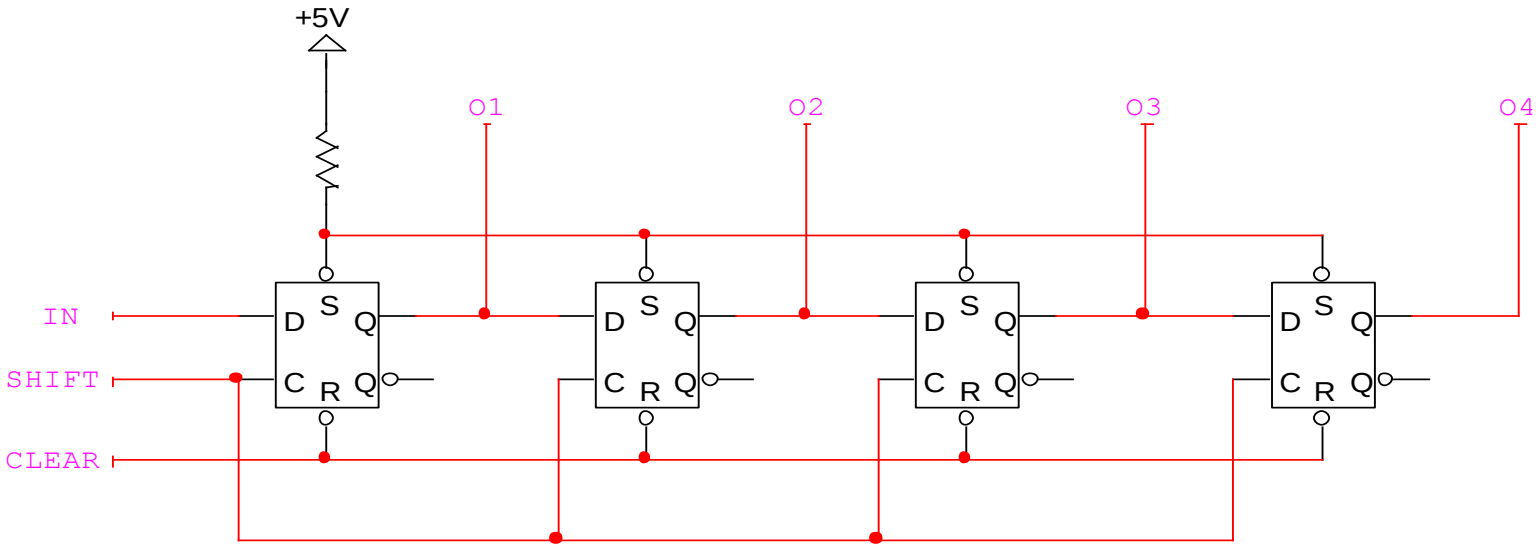


Basic Serial-In/Serial-Out Register



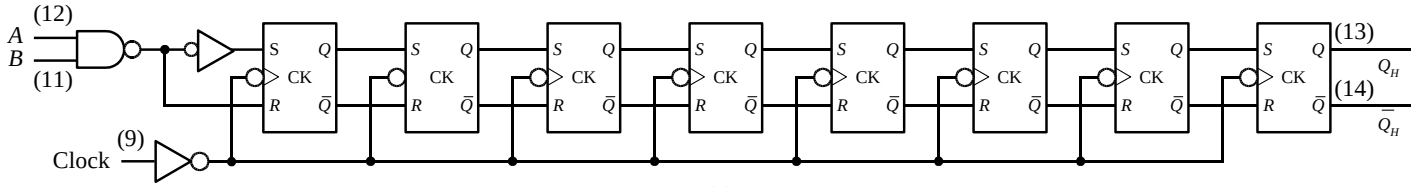


Four-Bit Shift Register Example



SHIFT	t0	t1	t2	t3	t4	t5	t6	t7	t8
IN	1	1	1	1	0	0	0	0	0
O1	0	1	1	1	1	0	0	0	0
O2	0	0	1	1	1	1	0	0	0
O3	0	0	0	1	1	1	1	0	0
O4	0	0	0	0	1	1	1	1	0

SN74491A Serial-in, Serial-out Shift Register



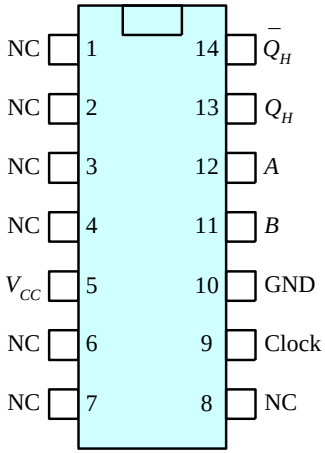
(a)

Inputs at t_n		Outputs at $t_n + 8$	
A	B	Q_H	$\bar{Q}_H$
H	H	H	L
L	×	L	H
×	L	L	H

$t_n + 8$ = Bit time after 8 low-to-high clock transitions

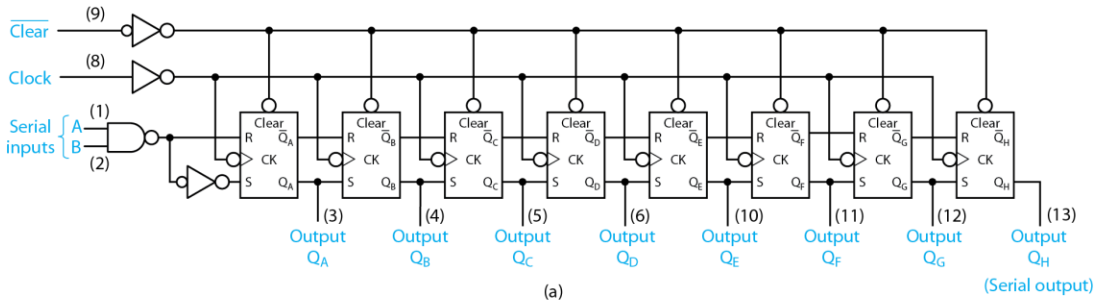
t_n = Reference bit time, clock low

(b)

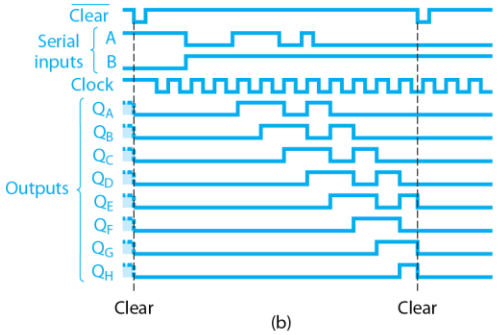


(c)

SN74164 Serial-in, Serial/Parallel-out Shift Register



(a)

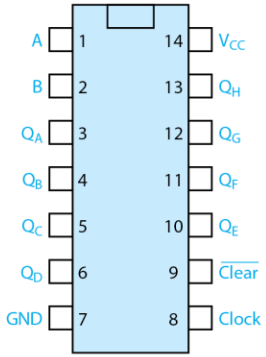


(b)

Inputs				Outputs			
$\overline{\text{Clear}}$	Clock	A	B	Q_A	Q_B	…	Q_H
L	¥	¥	¥	L	L		L
H	L	¥	¥	Q_{A0}	Q_{B0}		Q_{H0}
H	≠	H	H	H	Q_{An}		Q_{Gn}
H	≠	L	¥	L	Q_{An}		Q_{Gn}
H	≠	¥	L	L	Q_{An}		Q_{Gn}

Q_{A0}, Q_{B0}, Q_{H0} = levels of Q_A, Q_B, Q_H, respectively, before the indicated steady-state input conditions are established.
Q_{An}, Q_{Gn} = levels of Q_A, Q_G, respectively, before the most recent ≠ transition of the clock (1-bit shift)

(c)



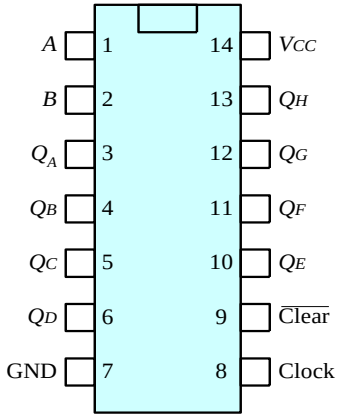
(d)

SN74164 Function Table and Package

Inputs				Outputs			
$\overline{\text{Clear}}$	Clock	A	B	QA	QB	É	QH
L	´	´	´	L	L		L
H	L	×	×	Q_{A0}	Q_{B0}		Q_{H0}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	×	L	Q_{An}		Q_{Gn}
H	↑	×	L	L	Q_{An}		Q_{Gn}

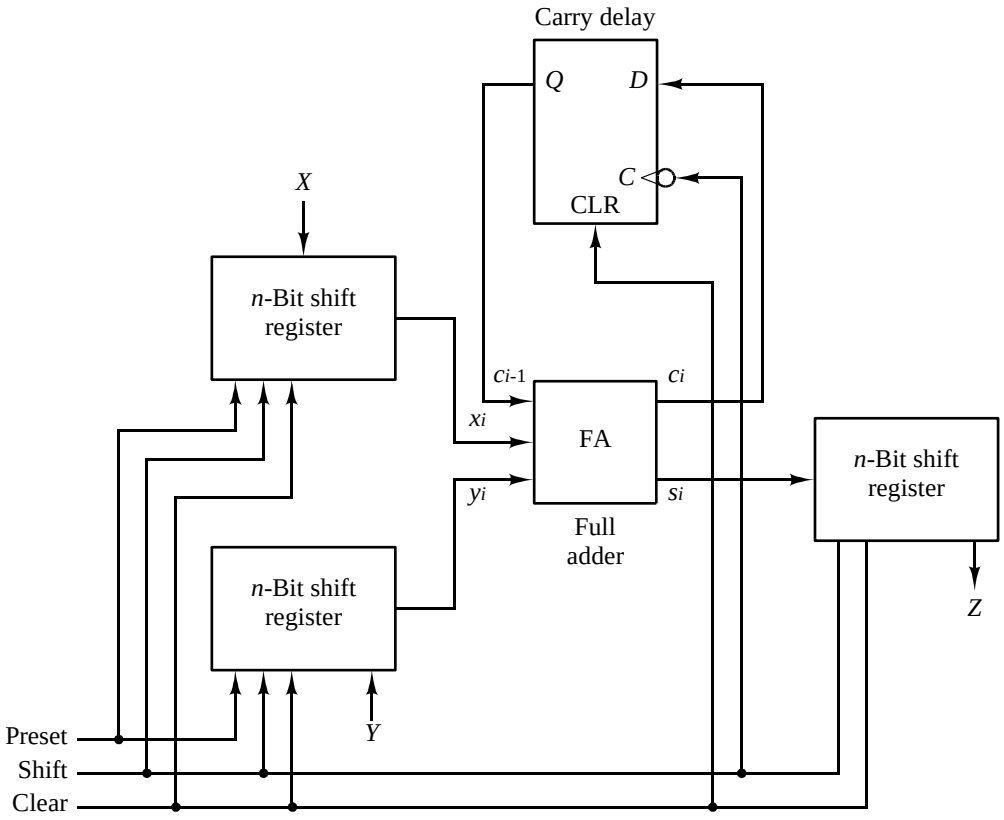
Q_{A0}, Q_{B0}, Q_{H0} = levels of Q_A, Q_B, Q_H, respectively, before the indicated steady-state input conditions are established.
Q_{An}, Q_{Gn} = levels of Q_A, Q_G, respectively, before the most recent - transition of the clock (1-bit shift)

(c)

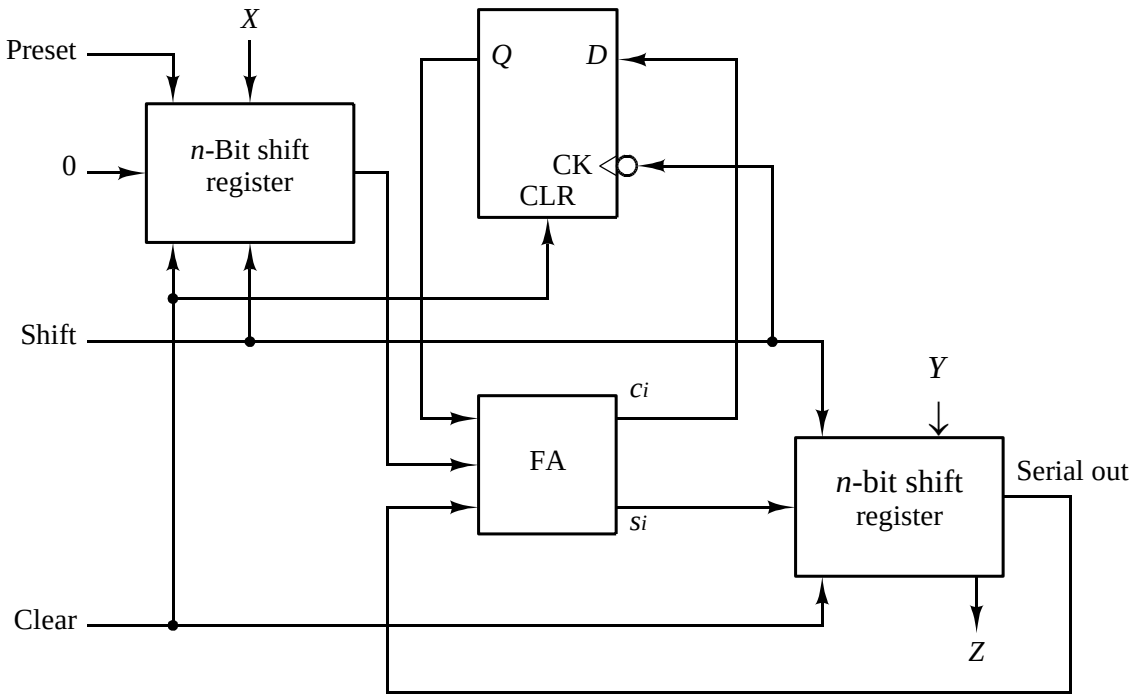


(d)

Serial Adder Unit

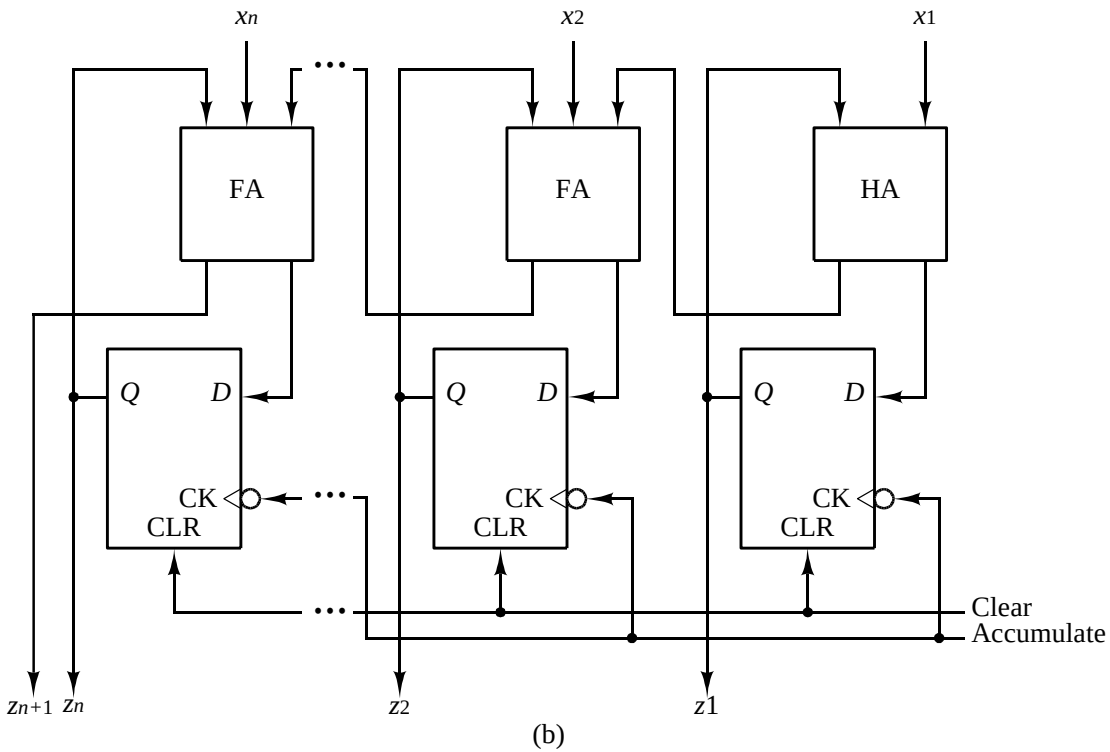


Serial Accumulator



(a)

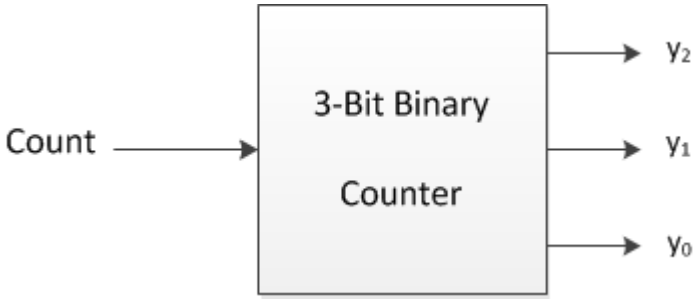
Parallel Accumulator

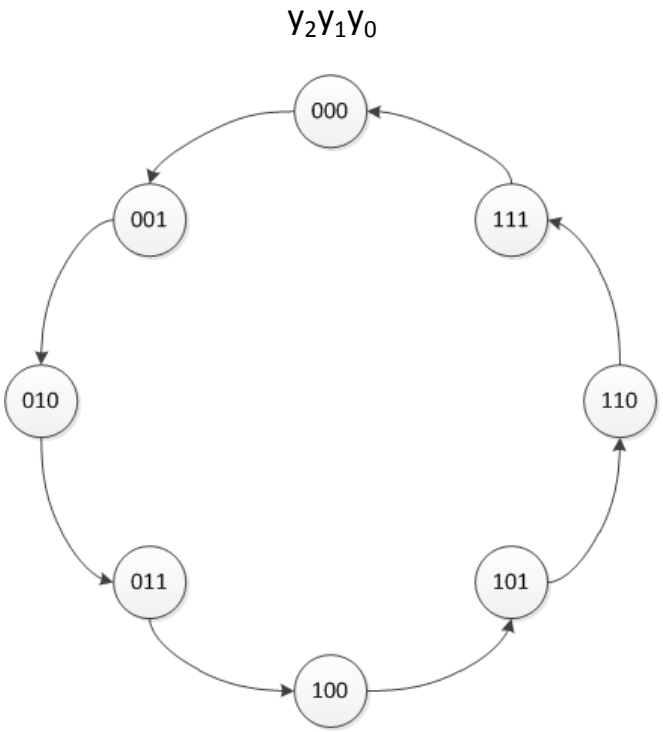


(b)

Introduction to Counters

- Counters – sequential circuits that tally, or count, in a predetermined code sequence, the number of input pulses received, e.g., 3-bit binary counter.

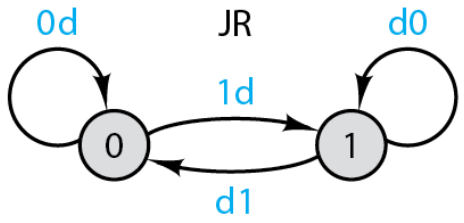




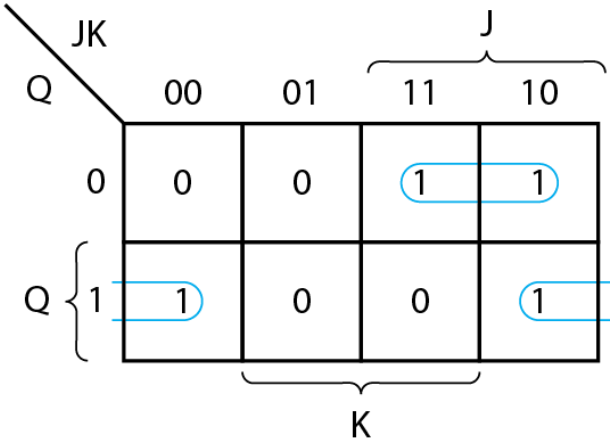
Recall How A JK Flip-flop Works

J	K	Q	C	Q*	
0	0	0	⎍	0	Hold
0	0	1	⎍	1	
0	1	0	⎍	0	Reset
0	1	1	⎍	0	
1	0	0	⎍	1	Set
1	0	1	⎍	1	
1	1	0	⎍	1	Toggle
1	1	1	⎍	0	

(a)

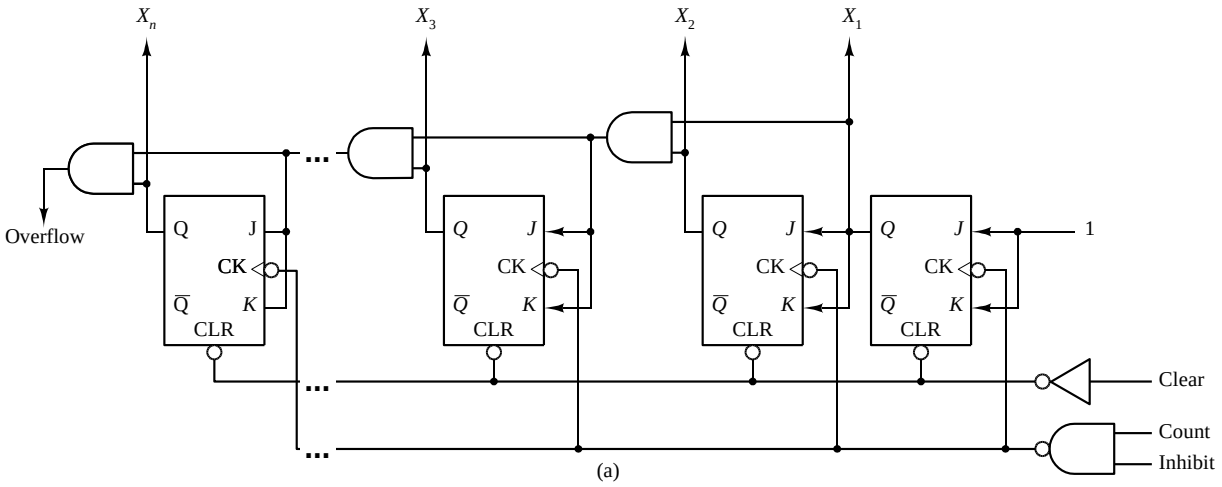


(b)



(c)

Synchronous Binary Counter



(a)

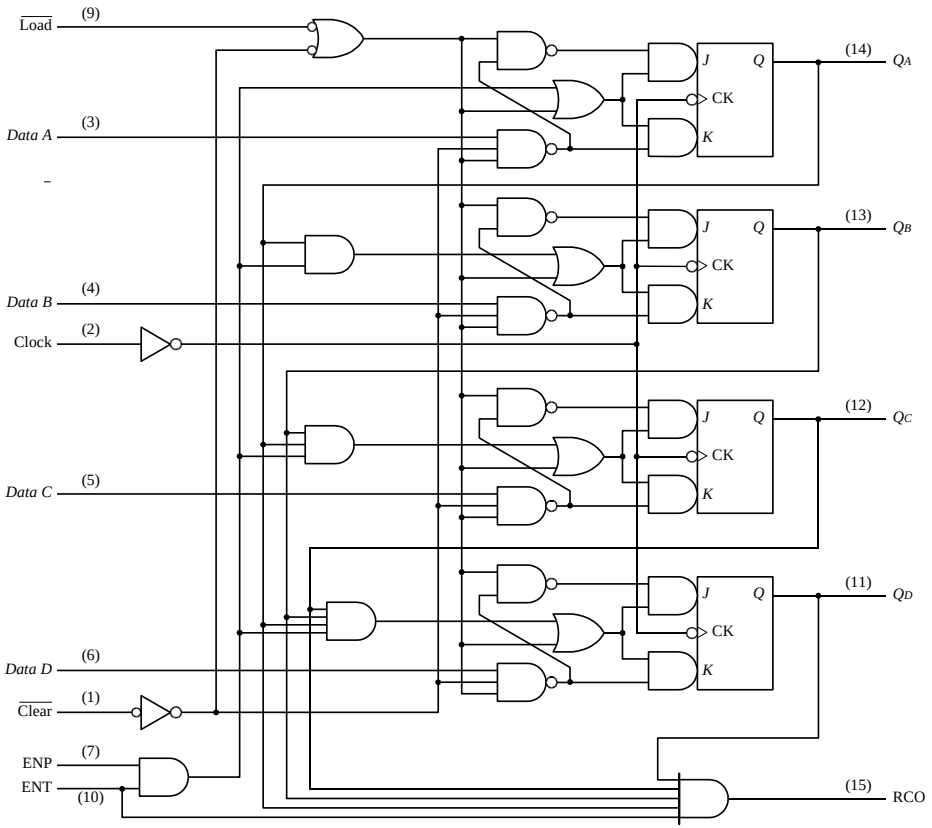
X_n	X_3	X_2	X_1	
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
1	1	1	0	
1	1	1	1	← Recycles
0	0	0	0	
0	0	0	1	
0	0	1	0	

(b)

Figure 7.11

X_4	X_3	X_2	X_1
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

SN74163 Synchronous Binary Counter



(a)

Inputs				
Clear	Load	ENT	ENP	Mode
L	↑	↑	↑	Synchronous clear
H	L	↑	↑	Synchronous load
H	H	H	H	Count
H	H	L	×	Hold
H	H	×	L	Hold

(b)

Figure 7.12

SN74163 Timing Diagram

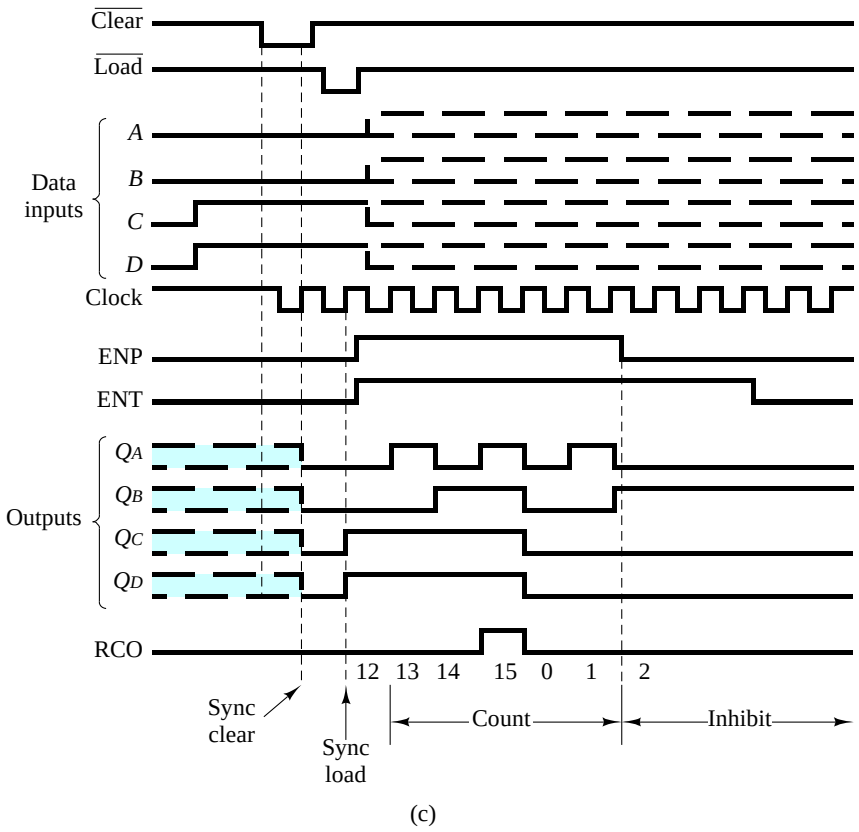


Figure 7.12, con't

Asynchronous Down Counter

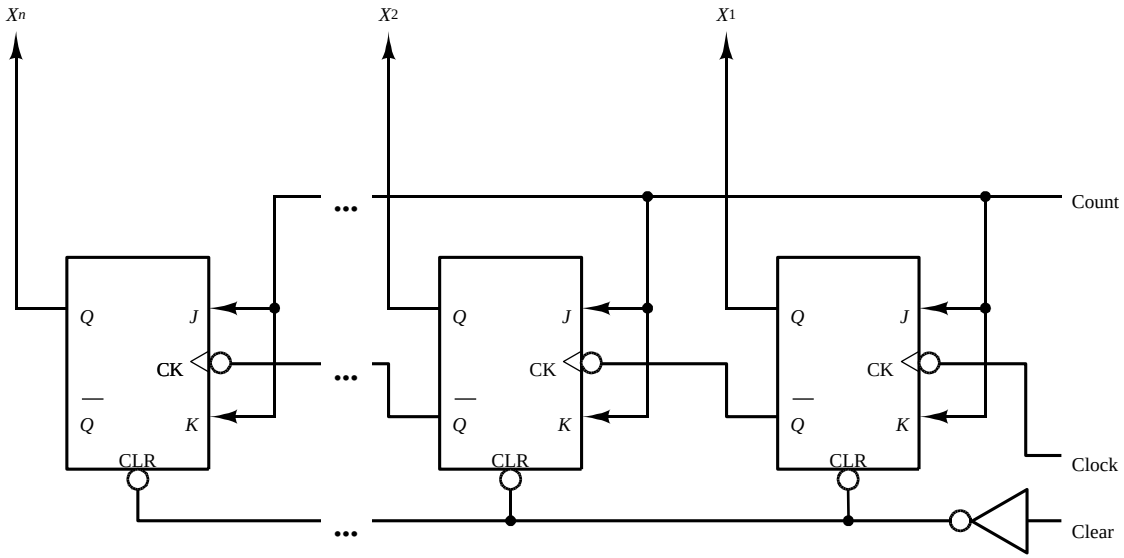
X_n	...	X_3	X_2	X_1
1	...	1	1	1
0	...	0	0	0
0	...	0	0	1
0	...	0	1	0
0	...	0	1	1
0	...	1	0	0

Up count mode

X_n	...	X_3	X_2	X_1
0	...	0	0	0
1	...	1	1	1
1	...	1	1	0
1	...	1	0	1
1	...	1	0	0
1	...	0	1	1

Down count mode

(a)



(b)

Figure 7.16

Synchronous Up/Down Counter

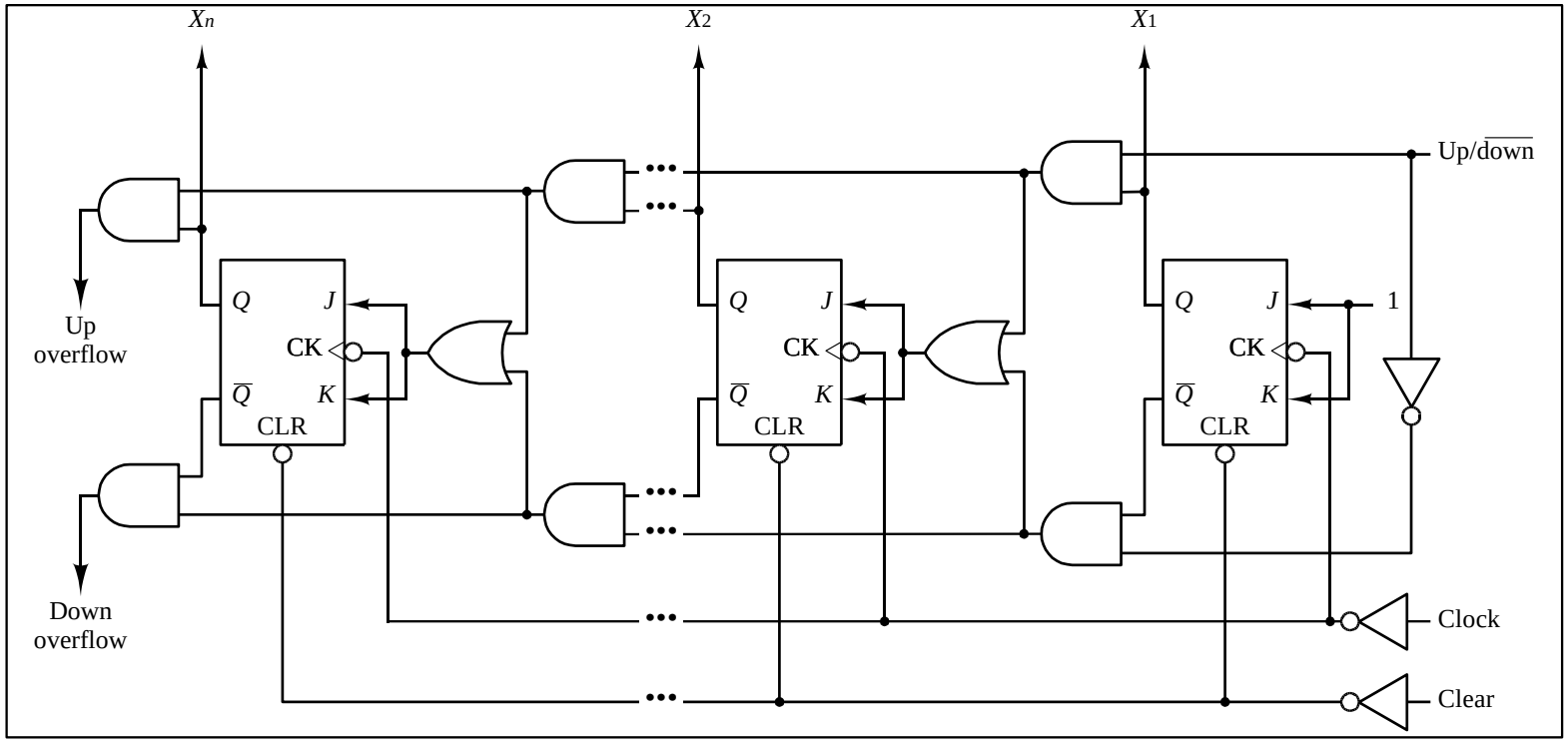
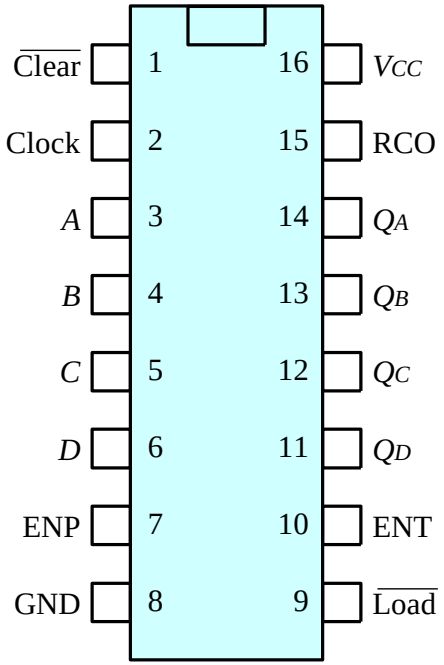


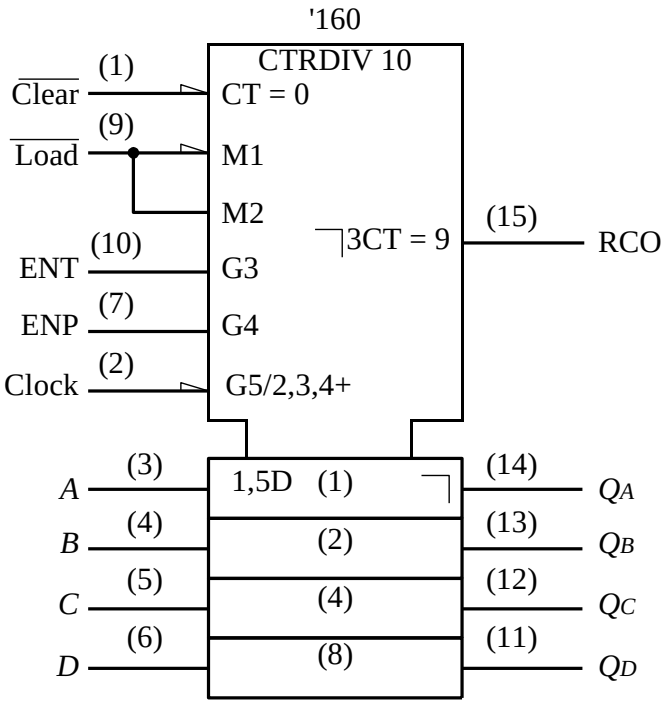
Figure 7.17

Modulo-*N* Counters – Counters that count from *0* to *N*-1 and repeat

- SN74160 Synchronous Decade Counter – counts *0* to *9*

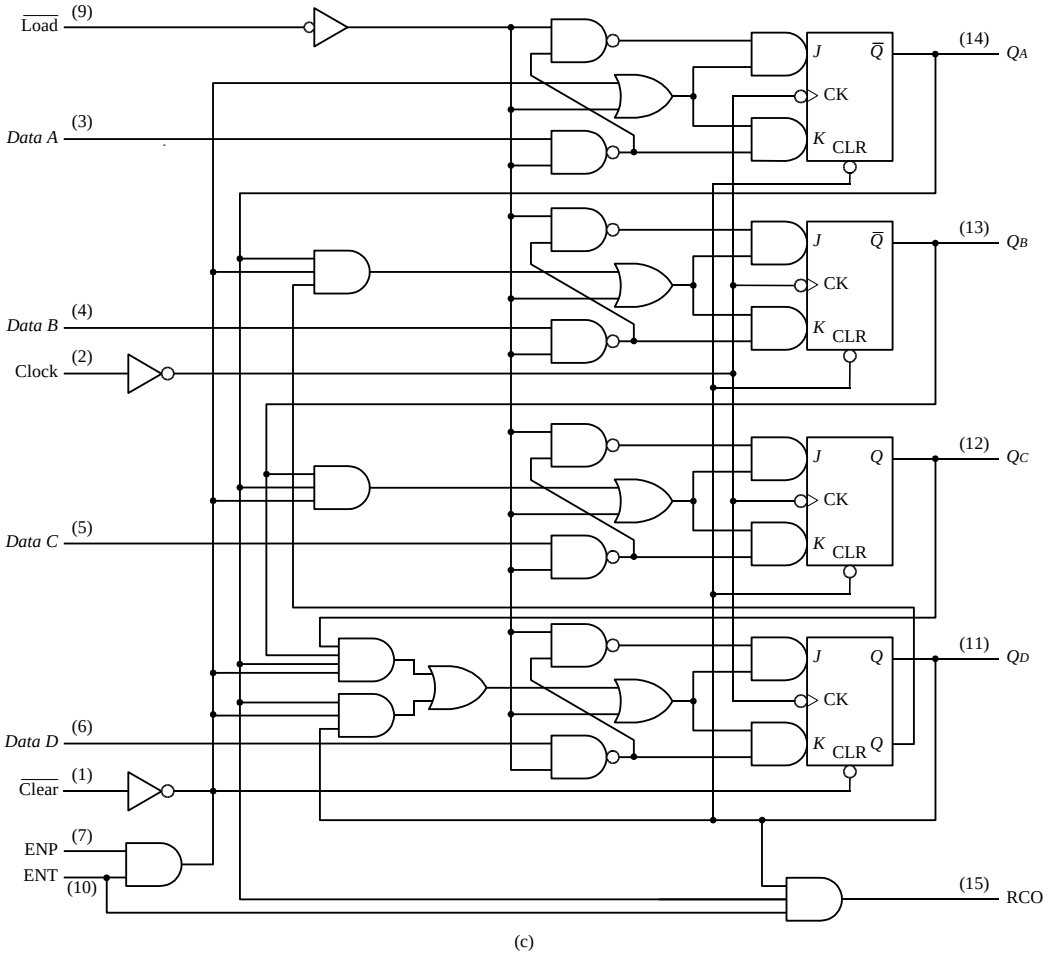


(a)



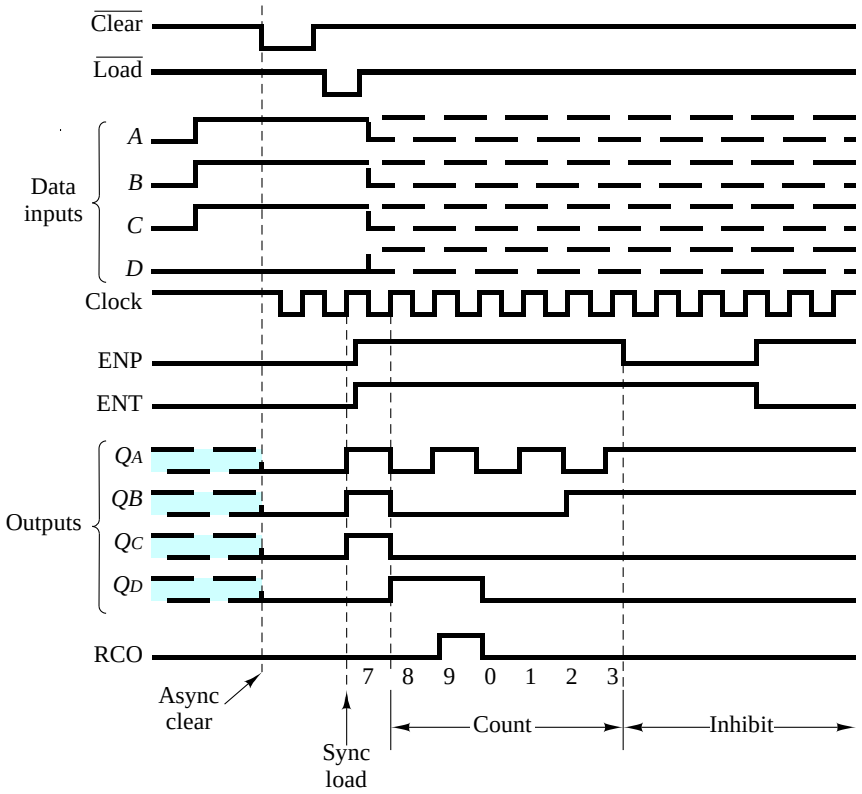
(b)

SN74160 Logic Diagram



(c)

SN74160 Timing Diagram



(d)

Digital Timer Block Diagram

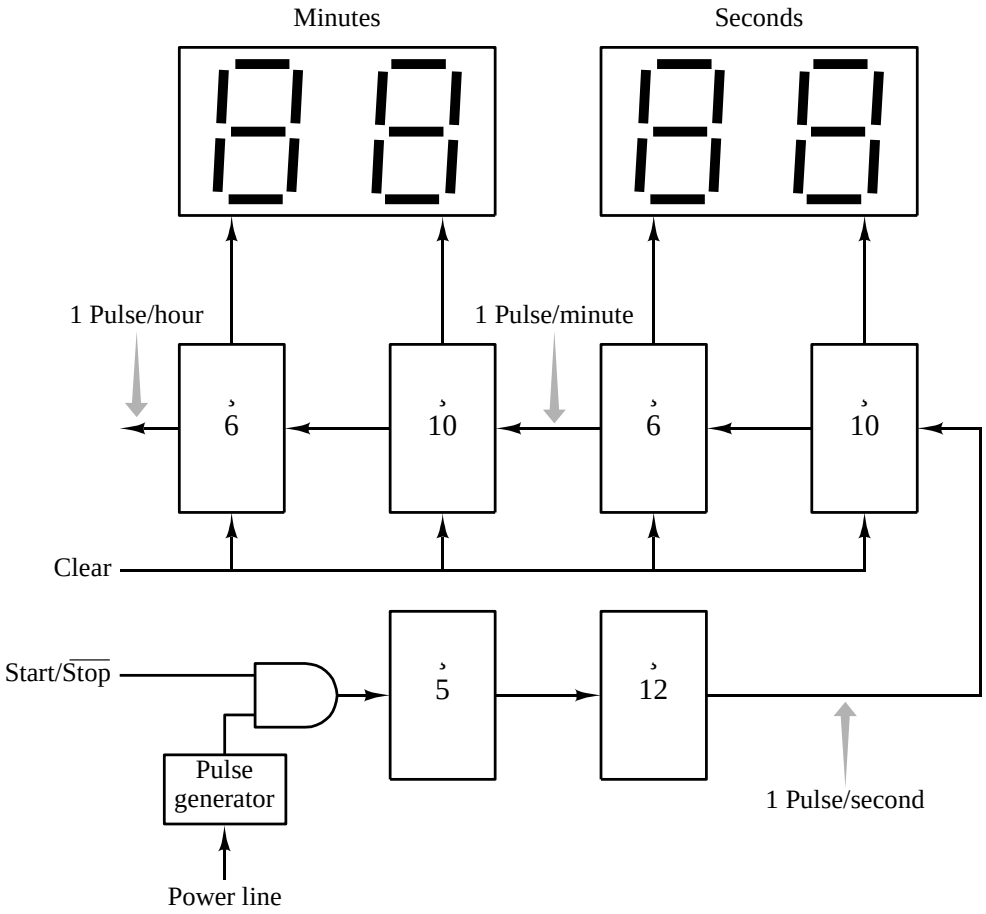
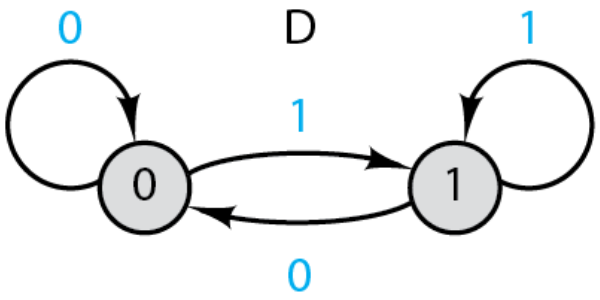


Figure 7.22

Recall D Flip Flop Functionality

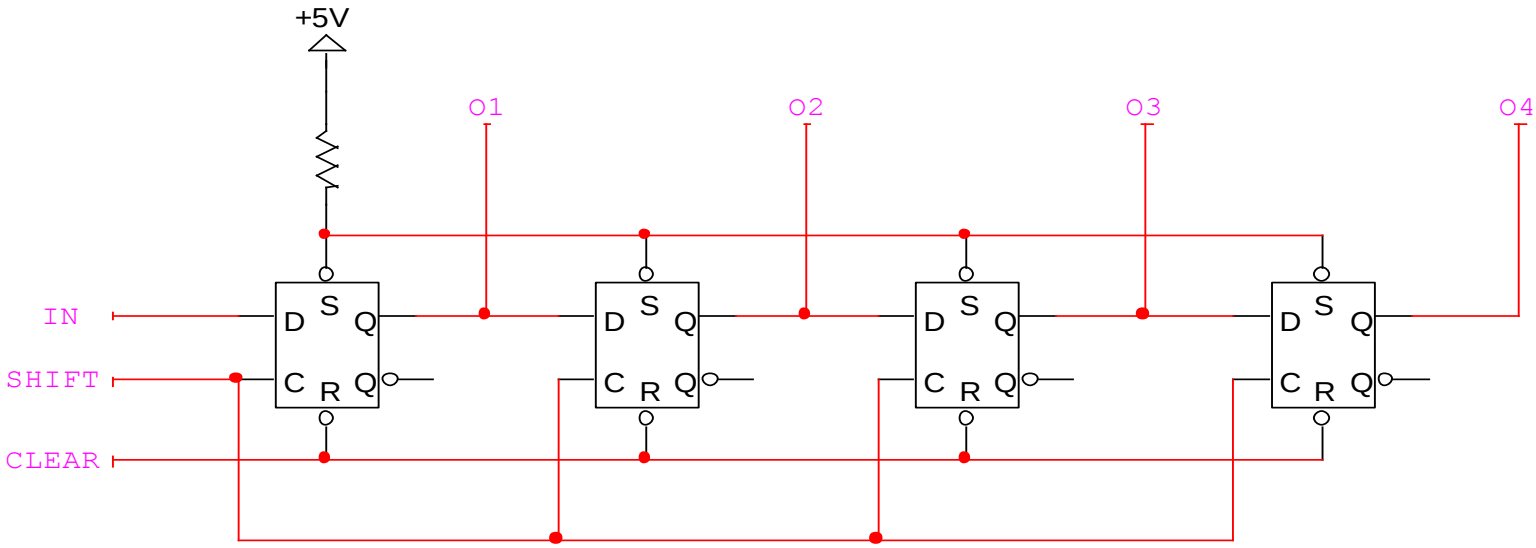
D	Q	C	Q*	
0	0	⊓	0	Store 0
0	1	⊓	0	
1	0	⊓	1	Store 1
1	1	⊓	1	

(a)



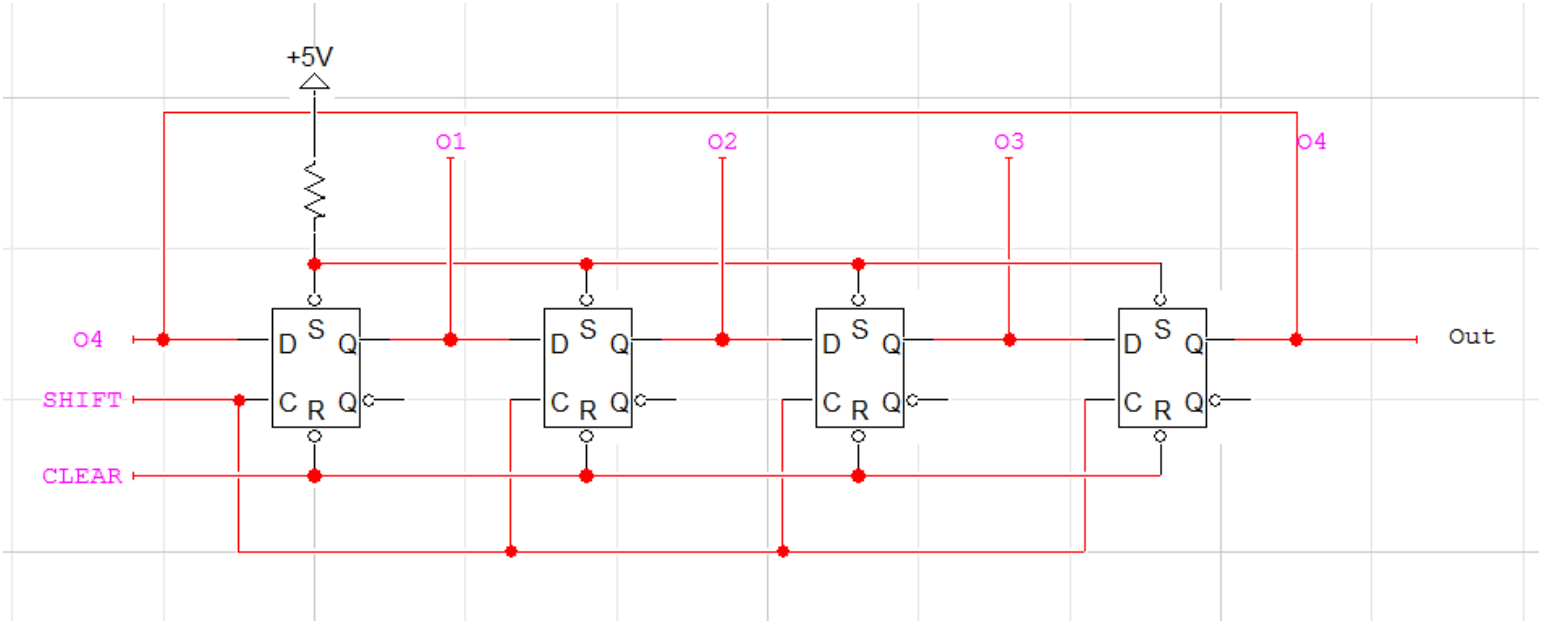
(b)

Four-Bit Shift Register Example



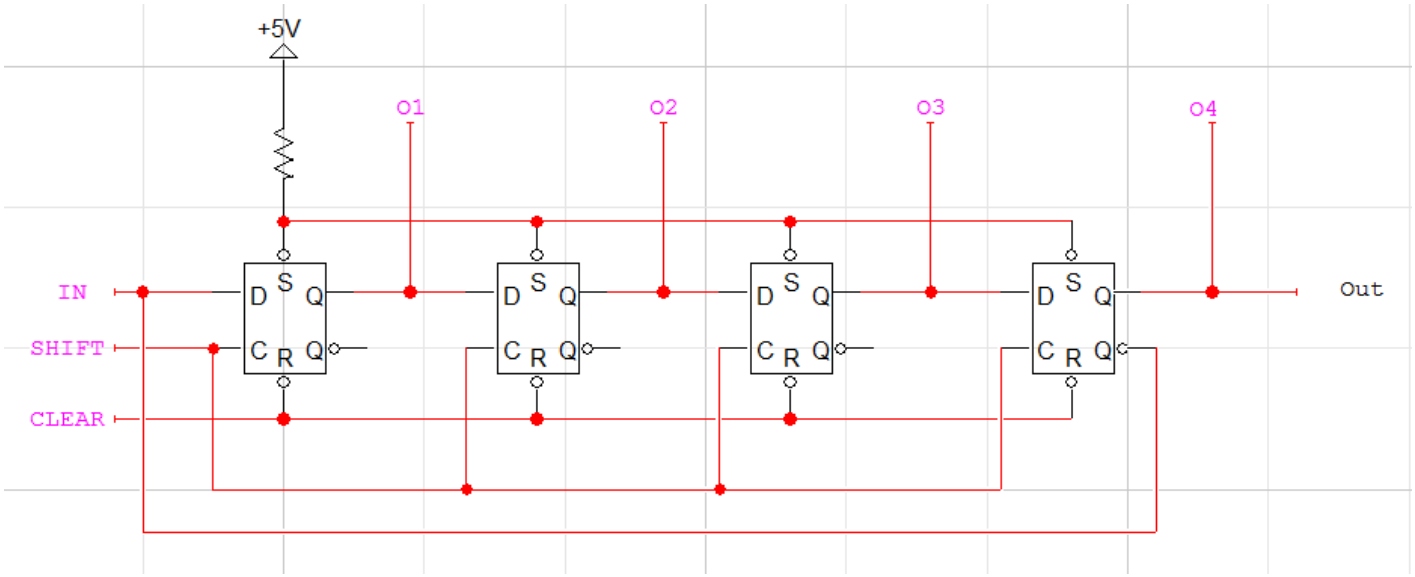
SHIFT	t0	t1	t2	t3	t4	t5	t6	t7	t8
IN	1	1	1	1	0	0	0	0	0
O1	0	1	1	1	1	0	0	0	0
O2	0	0	1	1	1	1	0	0	0
O3	0	0	0	1	1	1	1	0	0
O4	0	0	0	0	1	1	1	1	0

Four-Bit Ring Counter Example



SHIFT	t0	t1	t2	t3	t4	t5	t6	t7	t8
O1	1	0	0	0	1	0	0	0	1
O2	0	1	0	0	0	1	0	0	0
O3	0	0	1	0	0	0	1	0	0
O4	0	0	0	1	0	0	0	1	0

Four-Bit Twisted-Ring Counter



SHIFT	t0	t1	t2	t3	t4	t5	t6	t7	t8
IN	1	1	1	1	0	0	0	0	1
O1	0	1	1	1	1	0	0	0	0
O2	0	0	1	1	1	1	0	0	0
O3	0	0	0	1	1	1	1	0	0
O4	0	0	0	0	1	1	1	1	0