Multi-level circuits. Design Examples.
(Class 5.1 – 2/12/2013)

CSE 2441 – Introduction to Digital Logic

Spring 2013

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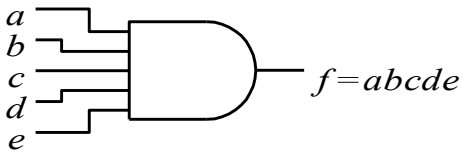
Today's Topics

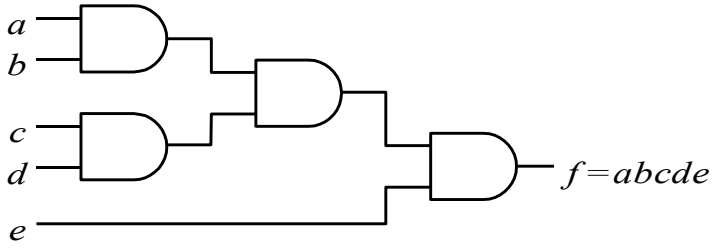
- Multi-level circuits
  - Fan-in constraints
  - Factoring
- Design examples

Synthesis of Combinational Logic Circuits (11)

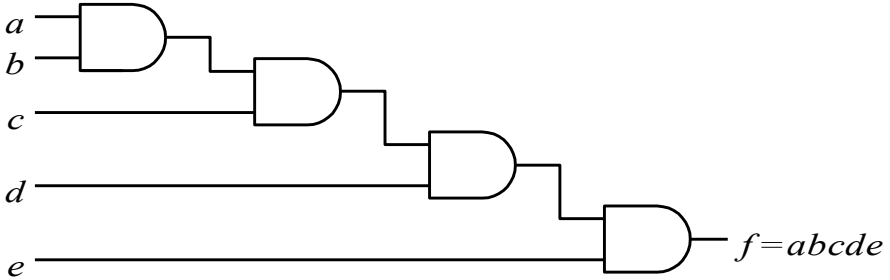
- Fan-in – the number of gate input lines (ports)
- Circuits with more than two levels are often needed due to fan-in, i.e., max number of input nodes, constraints of gates.



(a) A single five-input AND gate



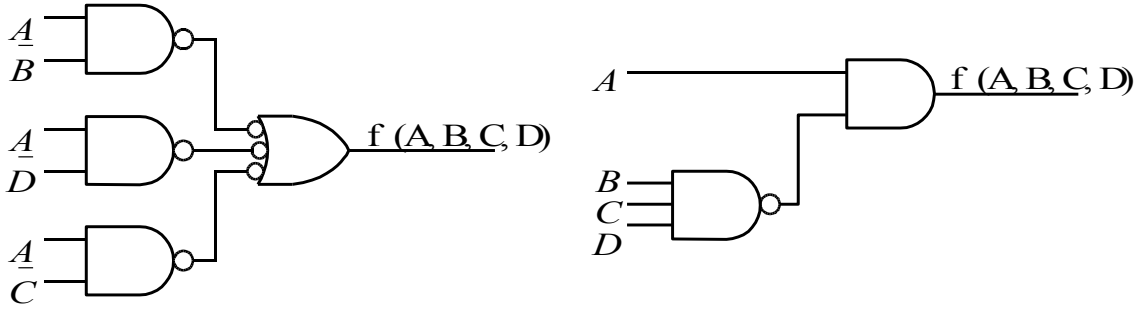
(b) Three-level network of two-input gates



(c) Four-level network of two-input gates.

Synthesis of Combinational Logic Circuits (12)

- ***Factoring***
  - A technique to obtain higher-level forms of switching functions.
  - Higher-level forms:
    - May need less hardware
    - May be used when there are fan-in constraints
    - More difficult to design
    - Slower
- ***Example 2.39***: $f(A,B,C,D) = A\overline{B} + A\overline{D} + A\overline{C} = A(\overline{B} + \overline{D} + \overline{C}) = A(\overline{BCD})$



(a) Original form (b) After factoring

Synthesis of Combinational Logic Circuits (13)

Example 2.40: Implement $f(a,b,c,d) = \Sigma m(8,13)$ with only two-input AND and OR gates.

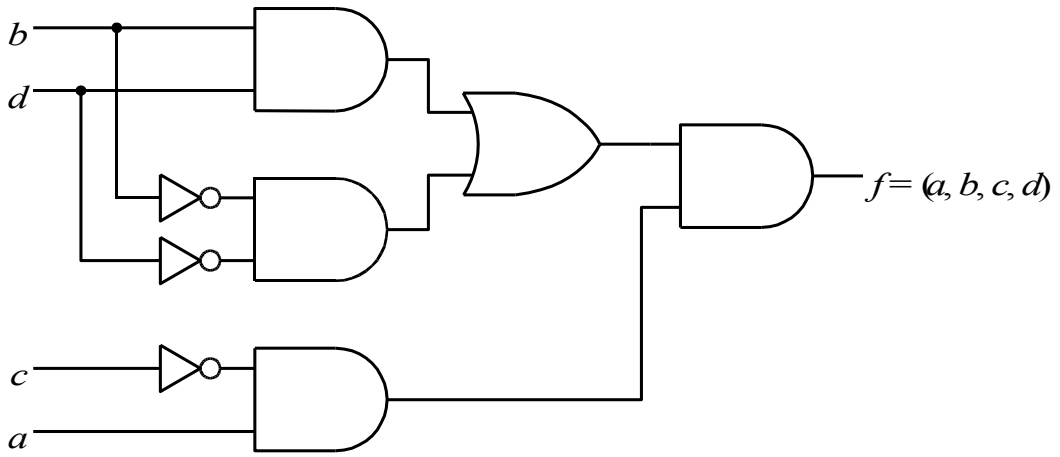
- Write the canonical SOP form:

  $f(a,b,c,d) = \Sigma m(8,13) = ab'c'd' + abc'd$ (2.34)

  Two four-input AND gates and one two-input OR gate are needed.

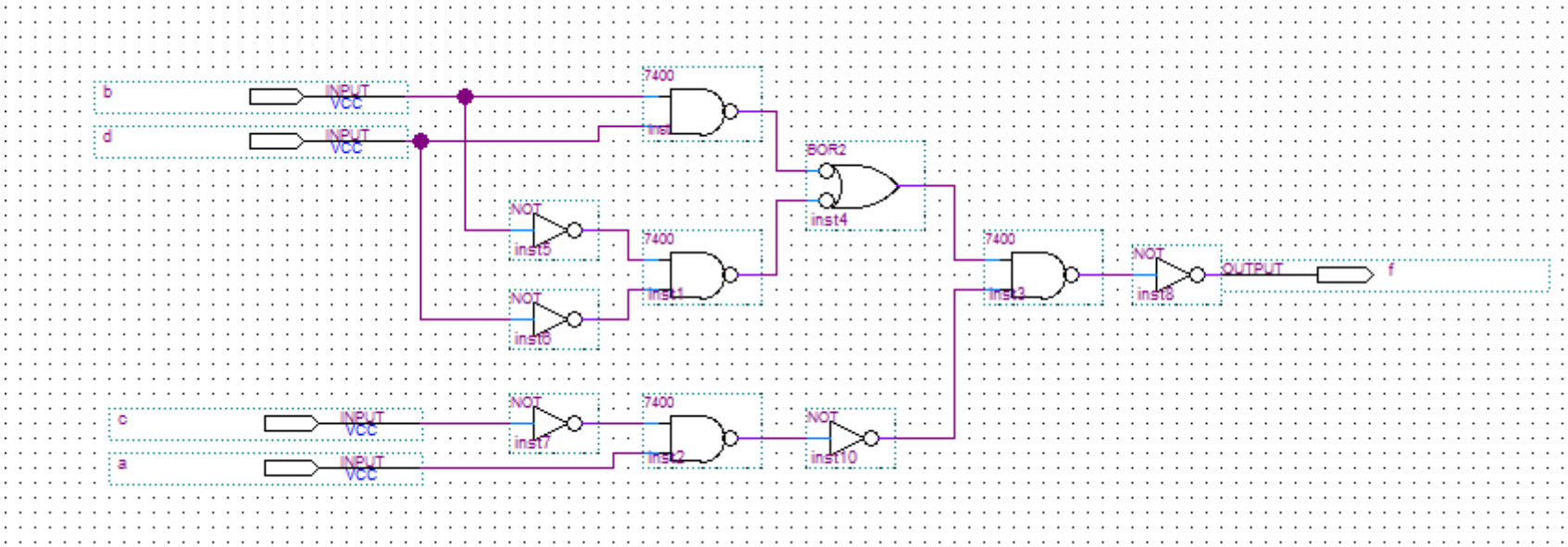
- Apply factoring:

$$f(a,b,c,d) = a\bar{b}\bar{c}\bar{d} + ab\bar{c}d = (a\bar{c})(bd + \bar{b}\bar{d}) \quad (2.35)$$



Synthesis of Combinational Logic Circuits (14)

- Convert the previous circuit to an all NAND realization.



Test Your Understanding

Implement the following function with only NAND2 gates.

$$f_{on}(A,B,C) = \sum m(2,3,4,5,7)$$

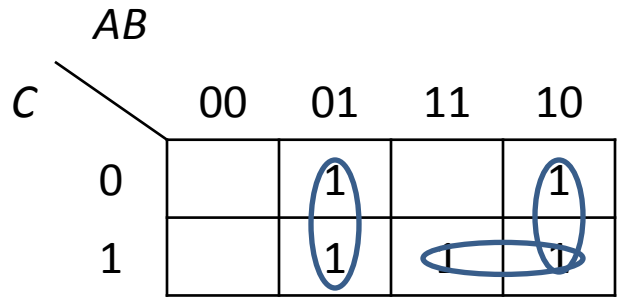
Assume all literals are available as inputs.

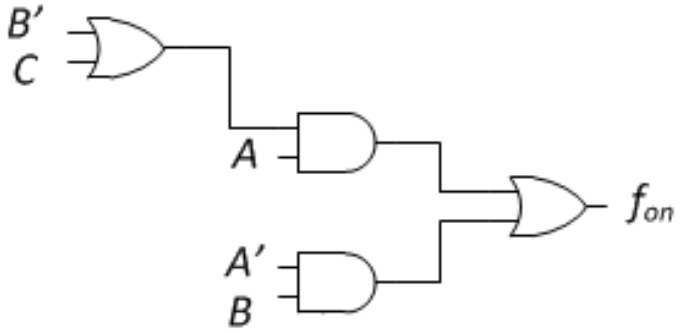
Test Your Understanding – Self-Check

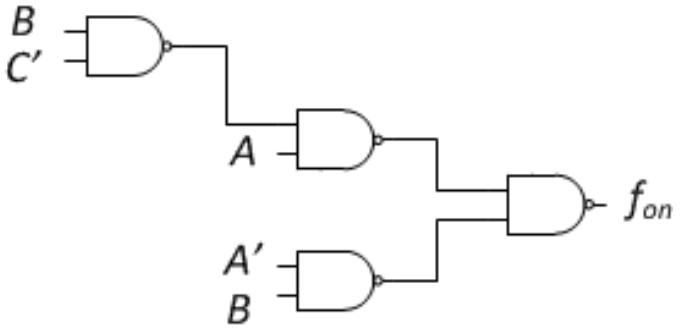
$f_{on}(A,B,C) = \sum m(2,3,4,5,7)$

$= A'B + AB' + AC$

$= A'B + A(B' + C)$







Design Example

The vault area of Unsecure Bank and Trust is secured by a lock that can be can be opened by bank officials according to the following protocol.

- During business hours – the bank president (P) or both of the vice presidents (VP1, VP2).
- Off hours – the president and either vice president.

Design a combinational logic circuit that will UNLOCK the lock when the appropriate combination of officials enter ID codes. Assume that logic 1 indicates that the proper code has been entered by the respective officer and that logic 0 means that the proper code was not entered. The variable OPEN=1 indicates that the bank is open for business.

Design Example – Develop a Truth Table

OPEN	*P*	*VP1*	*VP2*	*UNLOCK*
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Design Example – Derive Logic Equations

UNLOCK = $\sum m(5,6,7,11,12,13,14,15)$ [*Minterm list*]

$= O' \cdot P \cdot VP1' \cdot VP2 + O' \cdot P \cdot VP1 \cdot VP2' + O' \cdot P \cdot VP1 \cdot VP2$

$+ O \cdot P' \cdot VP1 \cdot VP2 + O \cdot P \cdot VP1' \cdot VP2' + O \cdot P \cdot VP1' \cdot VP2$

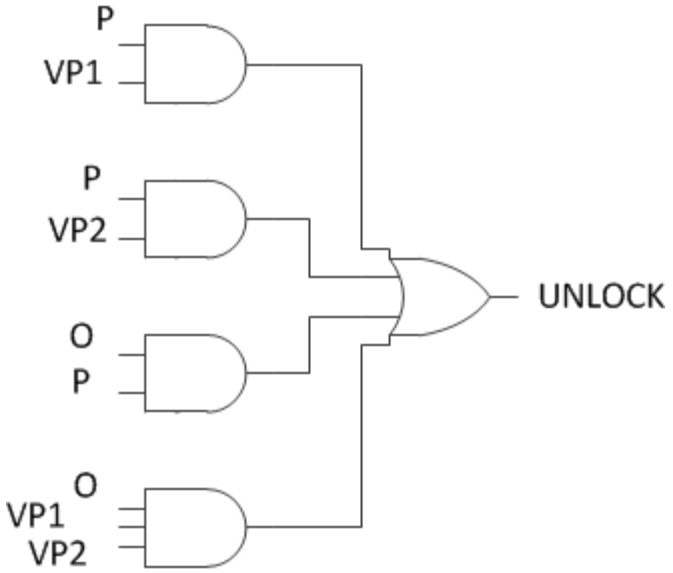
$+ O \cdot P \cdot VP1 \cdot VP2' + O \cdot P \cdot VP1 \cdot VP2$ [*CSP*]

$= P \cdot VP1 + P \cdot VP2 + O \cdot P + O \cdot VP1 \cdot VP2$ [*MSP*]

$= P(VP1+VP2) + O(P+VP1 \cdot VP2)$ [*Factored MSP*]

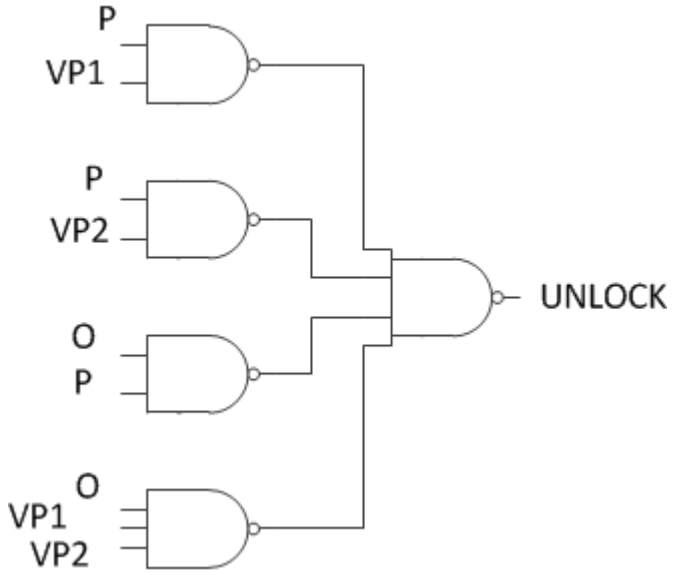
Design Example – Two-level Realizations

- AND/OR circuit



- Chips needed – SN7408, SN7411, 3xSN7432.

- NAND/NAND circuit

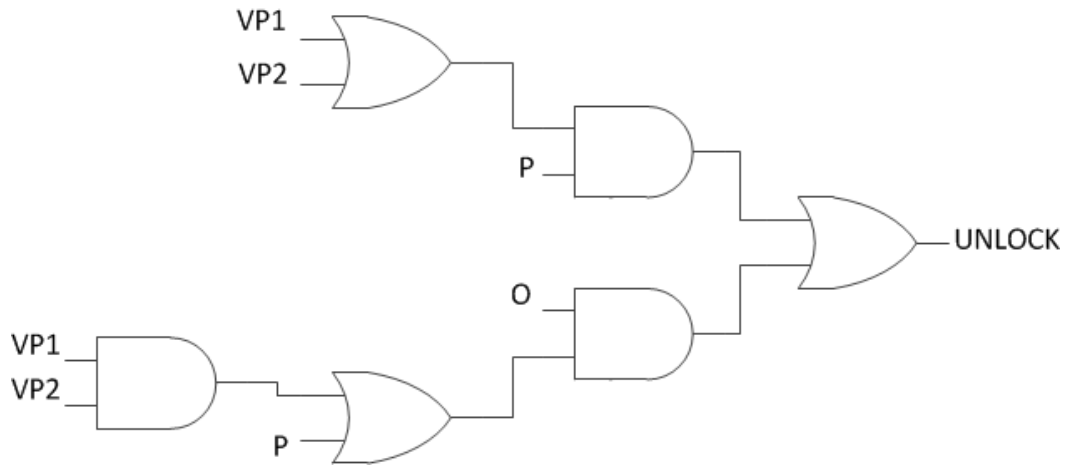


- Chips needed – SN7400, SN7420.

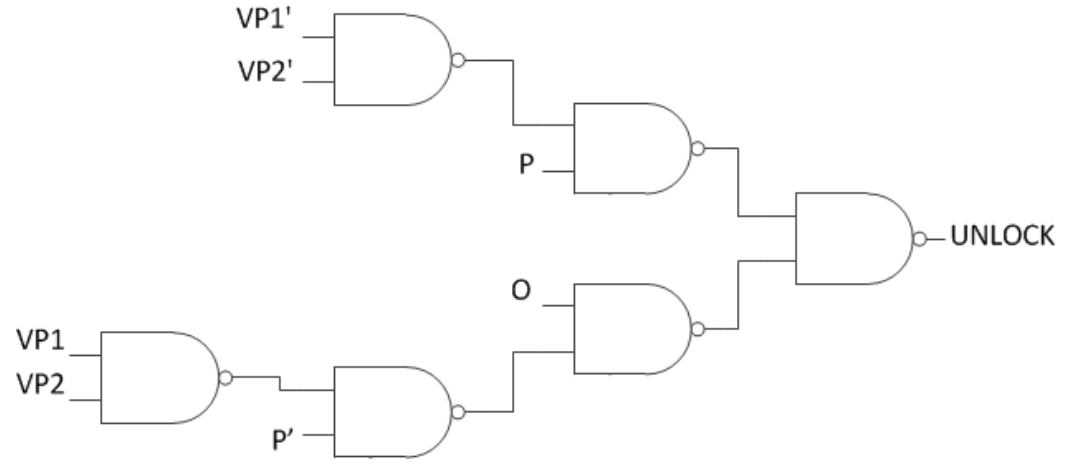
Maximum t_{pd} = 2Δ where Δ is the gate propagation delay.

Example – Multi-level Realizations

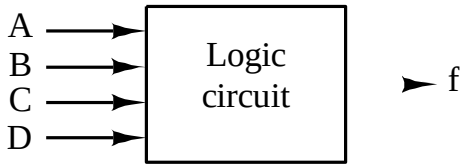
- AND, OR gates
  - Max t_{pd} = 4Δ
  - Chips needed
    - SN7408
    - SN7432



- All NAND gates
  - Max t_{pd} = 4Δ
  - Chips needed
    - 2xSN7400



Design a circuit to distinguish BCD digits ≥ 5 from those < 5



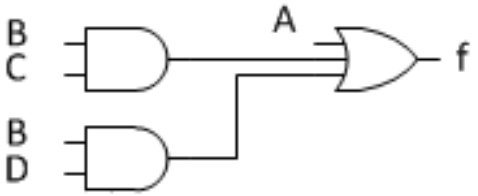
(a)

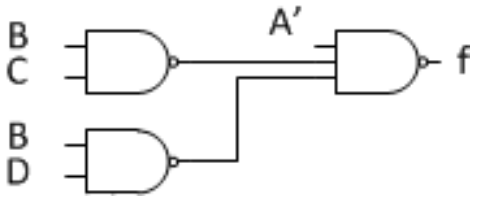
ABCD	Minterm	f(A, B, C, D)
0000	0	0
0001	1	0
0010	2	0
0011	3	0
0100	4	0
0101	5	1
0110	6	1
0111	7	1
1000	8	1
1001	9	1
1010	10	d
1011	11	d
1100	12	d
1101	13	d
1110	14	d
1111	15	d

(b)

Design a circuit to distinguish BCD digits ≥ 5 from those < 5 (con't)

$$f(A,B,C,D) = \sum m(5,6,7,8,9) + d(10,11,12,13,14,15)$$
$$= A + BC + BD$$





Design a circuit to distinguish BCD digits ≥ 5 from those < 5 (con't)

$$f(A,B,C,D) = A + BC + BD$$

$$= A + B(C + D)$$