

# Combinational Logic Circuit Analysis

(Class 3.1 – 9/11/12)

CSE 2441 – Introduction to Digital Logic  
Fall 2012

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# Today's Topics

- Boolean algebra (continued)
  - Product of sums forms
  - Incompletely specified functions
- Combinational logic circuit analysis
- Timing diagrams
- Gate delay

# Algebraic Forms of Switching Functions (5)

- A **maxterm** is a sum term in which all the variables appear exactly once either complemented or uncomplemented.
- **Canonical Product of Sums (canonical POS):**
  - Represented as a product of maxterms only.
  - **Example:**  $f_2(A,B,C) = (A+B+C)(A+B+C')(A'+B+C)(A'+B+C')$  (2.7)
- Maxterms of three variables:

Maxterm	Maxterm Code	Maxterm Number
$A+B+C$	000	$M_0$
$A+B+C'$	001	$M_1$
$A+B'+C$	010	$M_2$
$A+B'+C'$	011	$M_3$
$A'+B+C$	100	$M_4$
$A'+B+C'$	101	$M_5$
$A'+B'+C$	110	$M_6$
$A'+B'+C'$	111	$M_7$

# Algebraic Forms of Switching Functions (6)

- $f_2(A,B,C) = M_0M_1M_4M_5$  (2.8)

- $= \prod M(0,1,4,5)$  (maxterm list form) (2.9)

- The truth table for  $f_2(A,B,C)$ :

Rwo No. (i)	Inputs <i>ABC</i>	$M_0$ $A+B+C$	$M_1$ $A+B+C'$	$M_4$ $A'+B+C$	$M_5$ $A'+B+C'$	Outputs $f_2(A,B,C)$
0	000	0	1	1	1	0
1	001	1	0	1	1	0
2	010	1	1	1	1	1
3	011	1	1	1	1	1
4	100	1	1	0	1	0
5	101	1	1	1	0	0
6	110	1	1	1	1	1
7	111	1	1	1	1	1

# Algebraic Forms of Switching Functions (7)

- Truth tables of  $f_1(A,B,C)$  of Eq. (2.3) and  $f_2(A,B,C)$  of Eq. (2.7) are identical.

- Hence,  $f_1(A,B,C) = \Sigma m (2,3,6,7)$

$$= f_2(A,B,C)$$

$$= \Pi M(0,1,4,5)$$

(2.10)

- **Example: Given**  $f(A,B,C) = (A+B+C')(A+B'+C')(A'+B+C')(A'+B'+C')$ , construct the truth table and express in both maxterm and minterm form.

$$- f(A,B,C) = M_1M_3M_5M_7 = \Pi M(1,3,5,7) = \Sigma m (0,2,4,6)$$

Row No. (i)	Inputs ABC	Outputs $f(A,B,C) = \Pi M(1,3,5,7) = \Sigma m(0,2,4,6)$
0	000	1 <span style="float: right;"><math>m_0</math></span>
1	001	0 $\leftarrow M_1$
2	010	1 <span style="float: right;"><math>m_2</math></span>
3	011	0 $\leftarrow M_3$
4	100	1 <span style="float: right;"><math>m_4</math></span>
5	101	0 $\leftarrow M_5$
6	110	1 <span style="float: right;"><math>m_6</math></span>
7	111	0 $\leftarrow M_7$

# Algebraic Forms of Switching Functions (8)

- Relationship between minterm  $m_i$  and maxterm  $M_i$ :
  - For  $f(A,B,C)$ ,  $(m_1)' = (A'B'C)' = A + B + C' = M_1$
  - In general,  $(m_i)' = M_i$  (2.11)
  - $(M_i)' = ((m_i)')' = m_i$  (2.12)
- Example:** Relationship between the maxterms of a function and its complement. For  $f(A,B,C) = (A+B+C')(A+B'+C')(A'+B+C')(A'+B'+C')$ , the truth table is

Row No. (i)	Inputs ABC	Outputs $f(A,B,C)$	Outputs $f'(A,B,C) = \Pi M(0,2,4,6)$
0	000	1	0 $\leftarrow M_0$
1	001	0	1
2	010	1	0 $\leftarrow M_2$
3	011	0	1
4	100	1	0 $\leftarrow M_4$
5	101	0	1
6	110	1	0 $\leftarrow M_6$
7	111	0	1

# Algebraic Forms of Switching Functions (9)

- From the truth table

$$f'(A,B,C) = \prod M(0,2,4,6) \text{ and } f(A,B,C) = \prod M(1,3,5,7)$$

- Since  $f(A,B,C) \cdot f'(A,B,C) = 0$ ,

$$(M_0 M_2 M_4 M_6)(M_1 M_3 M_5 M_7) = 0 \text{ or } \prod_{i=0}^{2^3-1} M_i = 0$$

- In general,  $\prod_{i=0}^{2^n-1} M_i = 0$

(2.13)

- Another observation from the truth table:

$$f(A,B,C) = \sum m(0,2,4,6) = \prod M(1,3,5,7)$$

$$f'(A,B,C) = \sum m(1,3,5,7) = \prod M(0,2,4,6)$$

# Derivation of Canonical Forms (1)

- Derive canonical SOP or POS forms using switching algebra.

- **Theorem 10. Shannon's expansion theorem**

- (a).  $f(x_1, x_2, \dots, x_n) = x_1 f(1, x_2, \dots, x_n) + (x_1)' f(0, x_2, \dots, x_n)$

- (b).  $f(x_1, x_2, \dots, x_n) = [x_1 + f(0, x_2, \dots, x_n)] [(x_1)' + f(1, x_2, \dots, x_n)]$

- **Example:**  $f(A,B,C) = AB + AC' + A'C$

- $f(A,B,C) = AB + AC' + A'C = A f(1,B,C) + A' f(0,B,C)$

- $= A(1 \cdot B + 1 \cdot C' + 1' \cdot C) + A'(0 \cdot B + 0 \cdot C' + 0' \cdot C) = A(B + C') + A'C$

- $f(A,B,C) = A(B + C') + A'C = B[A(1+C')] + A'C] + B'[A(0 + C') + A'C]$

- $= B[A + A'C] + B'[AC' + A'C] = AB + A'BC + AB'C' + A'B'C$

- $f(A,B,C) = AB + A'BC + AB'C' + A'B'C$

- $= C[AB + A'B \cdot 1 + AB' \cdot 1' + A'B' \cdot 1] + C'[AB + A'B \cdot 0 + AB' \cdot 0' + A'B' \cdot 0]$

- $= ABC + A'BC + A'B'C + ABC' + AB'C'$



# Derivation of Canonical Forms (2)

- **Alternative:** Use Theorem 6 to add missing literals.
- **Example:**  $f(A,B,C) = AB + AC' + A'C$  to canonical SOP form.
  - $AB = ABC' + ABC = m_6 + m_7$
  - $AC' = AB'C' + ABC' = m_4 + m_6$
  - $A'C = A'B'C + A'BC = m_1 + m_3$
  - Therefore,  
$$f(A,B,C) = (m_6 + m_7) + (m_4 + m_6) + (m_1 + m_3) = \Sigma m(1, 3, 4, 6, 7)$$
- **Example:**  $f(A,B,C) = A(A + C')$  to canonical POS form.
  - $A = (A+B')(A+B) = (A+B'+C')(A+B'+C)(A+B+C')(A+B+C)$   
 $= M_3M_2M_1M_0$
  - $(A+C') = (A+B'+C')(A+B+C') = M_3M_1$
  - Therefore,  
$$f(A,B,C) = (M_3M_2M_1M_0)(M_3M_1) = \Pi M(0, 1, 2, 3)$$

# Incompletely Specified Functions

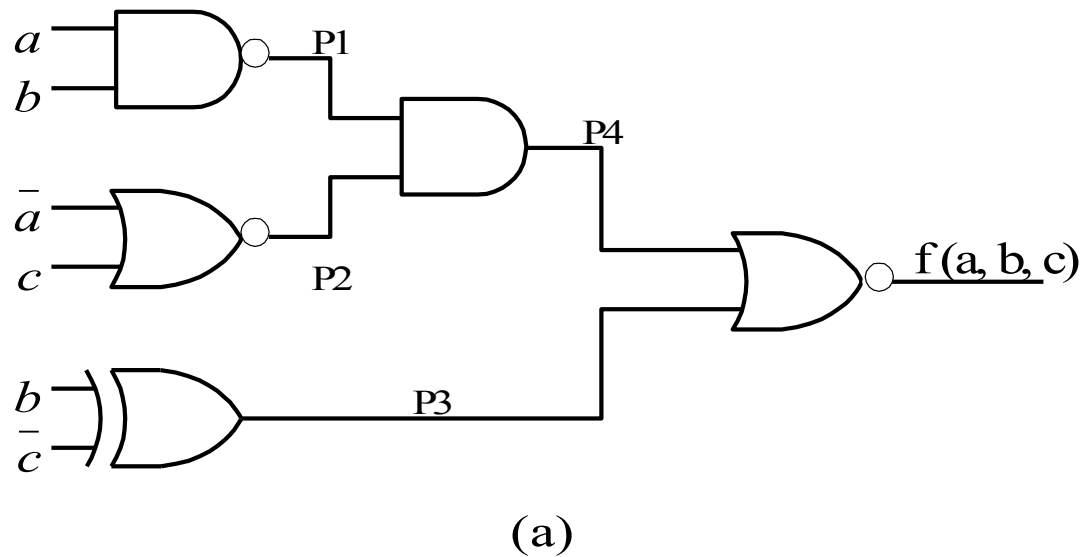
- A switching function may be incompletely specified.
- Some minterms are omitted, which are called *don't-care minterms*.
- When maxterms are omitted, they are called *don't-care maxterms*.
- Don't cares arise in two ways:
  - Certain input combinations never occur.
  - Output is required to be 1 or 0 only for certain combinations.
- Don't care minterms:  $d_i$       Don't care maxterms:  $D_i$
- **Example:**  $f(A,B,C)$  has minterms  $m_0, m_3,$  and  $m_7$  and don't-cares  $d_4$  and  $d_5$ .
  - Minterm list is:  $f(A,B,C) = \sum m(0,3,7) + d(4,5)$
  - Maxterm list is:  $f(A,B,C) = \prod M(1,2,6) \cdot D(4,5)$
  - $f'(A,B,C) = \sum m(1,2,6) + d(4,5) = \prod M(0,3,7) \cdot D(4,5)$
  - $f(A,B,C) = A'B'C' + A'BC + ABC + d(AB'C' + AB'C)$   
 $= B'C' + BC$  (use  $d_4$  and omit  $d_5$ )

# Analysis of Combinational Circuits (1)

- Digital Circuit **Design**:
  - Word description of a function
    - ⇒ a set of switching equations
    - ⇒ hardware realization (gates, programmable logic devices, etc.)
- Digital Circuit **Analysis**:
  - Hardware realization
    - ⇒ switching expressions, truth tables, timing diagrams, etc.
- Analysis is used
  - To determine the behavior of the circuit
  - To verify the correctness of the circuit
  - To assist in converting the circuit to a different form.

# Analysis of Combinational Circuits (2)

- **Algebraic Method:** Use switching algebra to derive a desired form.
- **Example 2.33:** Find a simplified switching expressions and logic circuit for the following circuit (Fig. 2.21a).



# Analysis of Combinational Circuits (3)

- Write switching expression for each gate output:  
 $P_1 = \overline{ab}$ ,  $P_2 = \overline{a+c}$ ,  $P_3 = b \oplus \overline{c}$ ,  $P_4 = P_1 \cdot P_2 = \overline{ab} \cdot \overline{(a+c)}$
- The output is:  $f(a,b,c) = \overline{P_3 + P_4} = \overline{(b \oplus \overline{c}) + \overline{ab} \cdot \overline{(a+c)}}$
- Simplify the output function using switching algebra:

$$\begin{aligned} \overline{f(a,b,c)} &= \overline{(b \oplus \overline{c}) + \overline{ab} \cdot \overline{a+c}} \\ &= bc + \overline{b}\overline{c} + \overline{ab} \cdot \overline{a+c} \end{aligned} \quad [\text{Eq. 2.24}]$$

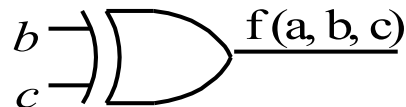
$$= bc + \overline{b}\overline{c} + (\overline{a} + \overline{b})a\overline{c} \quad [\text{T8}]$$

$$= bc + \overline{b}\overline{c} + \overline{a}a\overline{c} + b\overline{a}\overline{c} \quad [\text{T5(b)}]$$

$$= bc + \overline{b}\overline{c} \quad [\text{T4(a)}]$$

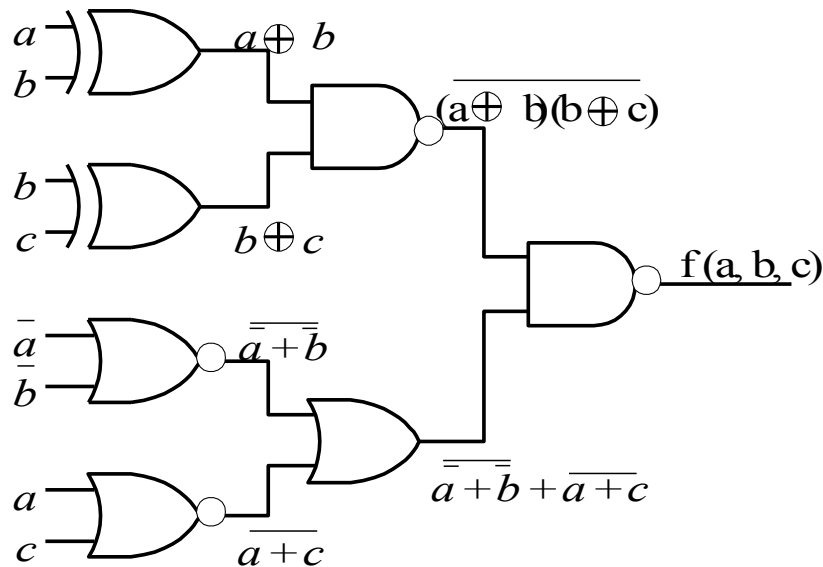
$$\overline{f(a,b,c)} = b \odot c \quad [\text{Eq. 2.32}]$$

Therefore,  $f(a,b,c) = (b \odot c)' = b \oplus c$



# Analysis of Combinational Circuits (4)

- Example 2.34:** Find a simplified switching expression and logic network for the following logic circuit (Fig. 2.22).

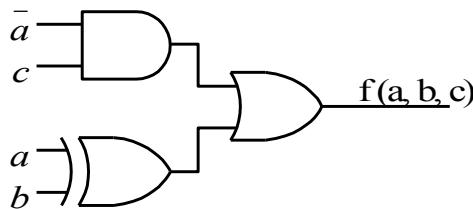


Given circuit

# Analysis of Combinational Circuits (5)

- Derive the output expression:

$$\begin{aligned}
 f(a,b,c) &= \overline{\overline{(a \oplus b)(b \oplus c)} \cdot \overline{\overline{(\bar{a} + \bar{b} + a + c)}}} \\
 &= \overline{(a \oplus b)(b \oplus c) + \bar{a} + \bar{b} + a + c} && \text{[T8(b)]} \\
 &= (a \oplus b)(b \oplus c) + (\bar{a} + \bar{b})(a + c) && \text{[T8(a)]} \\
 &= (a\bar{b} + \bar{a}b)(b\bar{c} + \bar{b}c) + (\bar{a} + \bar{b})(a + c) && \text{[Eq. 2.24]} \\
 &= a\bar{b}\bar{b}\bar{c} + a\bar{b}\bar{b}c + \bar{a}b\bar{b}\bar{c} + \bar{a}b\bar{b}c + \bar{a}a + \bar{a}c + a\bar{b} + \bar{b}c && \text{[P5(b)]} \\
 &= a\bar{b}c + \bar{a}b\bar{c} + \bar{a}c + a\bar{b} + \bar{b}c && \text{[P6(b), T4(a)]} \\
 &= \bar{a}b\bar{c} + \bar{a}c + a\bar{b} + \bar{b}c && \text{[T4(a)]} \\
 &= \bar{a}b\bar{c} + \bar{a}c + a\bar{b} && \text{[T9(a)]} \\
 &= \bar{a}b + \bar{a}c + a\bar{b} && \text{[T7(a)]} \\
 &= \bar{a}c + a \oplus b && \text{[Eq. 2.24]}
 \end{aligned}$$



Simplified circuit

# Analysis of Combinational Circuits (6)

- ***Truth Table Method***: Derive the truth table one gate at a time.
- The truth table for Example 2.34:

$abc$	$\bar{a}c$	$a \oplus b$	$f(a,b,c)$
000	0	0	0
001	1	0	1
010	0	1	1
011	1	1	1
100	0	1	1
101	0	1	1
110	0	0	0
111	0	0	0

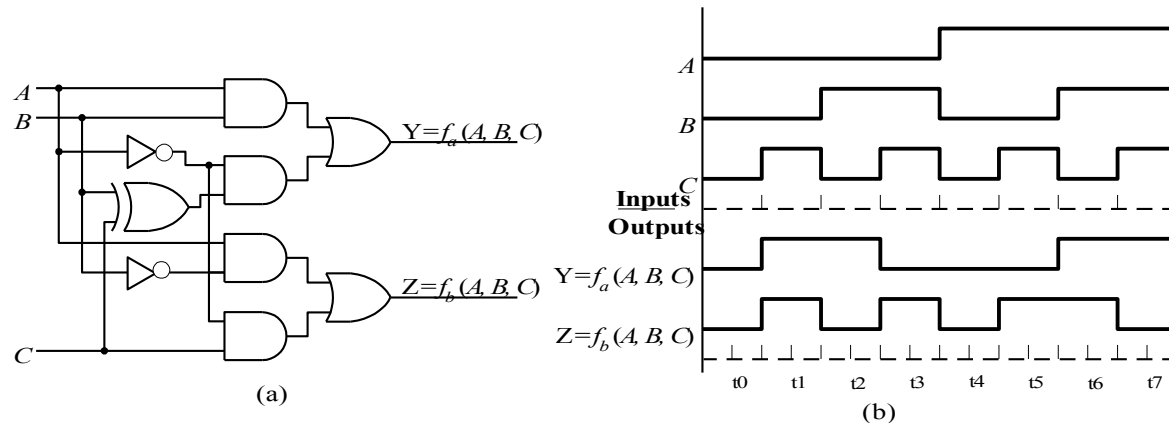


# Analysis of Combinational Circuits (7)

- ***Analysis of Timing Diagrams***
  - The *Timing diagram* is a graphical representation of input and output signal relationships over time.
  - Timing diagrams may show intermediate signals and propagation delays.

# Analysis of Combinational Circuits (8)

- **Example 2.35:** Derivation of truth table from a timing diagram



Time	Inputs	Outputs	
	$ABC$	$f_a(A, B, C)$	$f_b(A, B, C)$
$t_0$	0 0 0	0	0
$t_1$	0 0 1	1	1
$t_2$	0 1 0	1	0
$t_3$	0 1 1	0	1
$t_4$	1 0 0	0	0
$t_5$	1 0 1	0	1
$t_6$	1 1 0	1	1
$t_7$	1 1 1	1	0

(c)

# Analysis of Combinational Circuits (9)

- ***Propagation Delay***

- Physical characteristics of a logic circuit to be considered:

- Propagation delays
- Gate fan-in and fan-out restrictions
- Power consumption
- Size and weight

- *Propagation delay*: The delay between the time of an input change and the corresponding output change.

- Typical two propagation delay parameters:

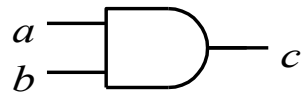
- $t_{PLH}$  = propagation delay time, low-to-high-level output
- $t_{PHL}$  = propagation delay time, high-to-low-level output

- Approximation:

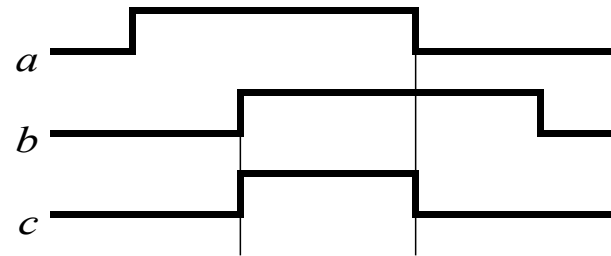
$$t_{PD} = \frac{t_{PLH} + t_{PHL}}{2}$$

# Analysis of Combinational Circuits (10)

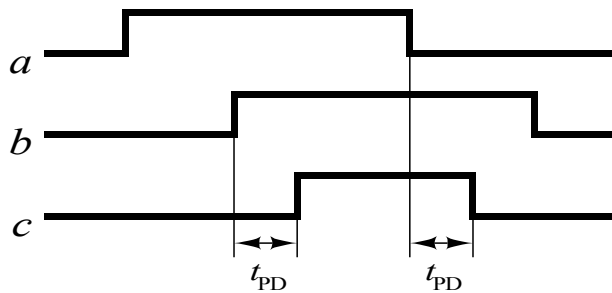
- Propagation delay through a logic gate



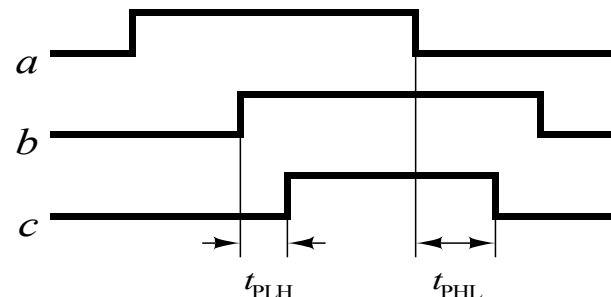
(a) Two-input AND gate



(b) Ideal (zero) delay



(c)  $t_{PD} = t_{PLH} = t_{PHL}$



(d)  $t_{PLH} < t_{PHL}$

# Analysis of Combinational Circuits (11)

- Power dissipation and propagation delays for several logic families (Table 2.7)

Logic Family	Propagation Delay $t_{PD}$ (ns)	Power Dissipation Per Gate (mW)	Technology
7400	10	10	Standard TTL
74H00	6	22	High-speed TTL
74L00	33	1	Low-power TTL
74LS00	9.5	2	Low-power Schottky TTL
74S00	3	19	Schottky TTL
74ALS00	3.5	1.3	Advanced low-power Schottky TTL
74AS00	3	8	Advanced Schottky TTL
74HC00	8	0.17	High-speed CMOS

# Analysis of Combinational Circuits (12)

- Propagation delays of primitive 74LS series gates (Table 2.8)

Chip	Function	$t_{PLH}$		$t_{PHL}$	
		Typical	Maximum	Typical	Maximum
74LS04	NOT	9	15	10	15
74LS00	NAND	9	15	10	15
74LS02	NOR	10	15	10	15
74LS08	AND	8	15	10	20
74LS32	OR	14	22	14	22