Name: _____ ID# _____

Date Submitted: _____ Lab Section # _____

CSE 2441 – Introduction to Digital Logic Spring Semester 2013

Lab Number 9 – Binary To Two's Complement Converter

To be performed the weeks of April 1 and 8, 2013.

Note: You will not be given any extra time to complete this lab. So use your time wisely.

CSE 2441 **LABORATORY ASSIGNMENT 9** **SPRING 2013**

BINARY TO TWO'S COMPLEMENT CONVERTER

(150 POINTS)

PURPOSE/OUTCOMES:

To design, implement on the DE1, and test a Mealy type sequential circuit that recognizes sequences of three-bit serial binary code words and converts each word to its two's complement. Once you complete this assignment, you will have demonstrated an ability to design a sequential circuit that meets specified requirements and to implement the design on a Cyclone II field programmable gate array (FPGA).

BACKGROUND:

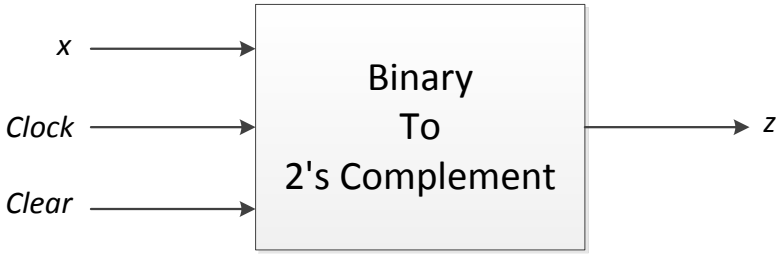
Sequential circuits can be used as sequence recognizers and, hence, can be designed to function as code converters. Sequences can be considered as block or non-block codes. Block codes have a fixed length and are not overlapping for recognition purposes. A non-block code has no fixed length and may contain overlapping segments. For example consider the three-bit code word 101. The sequence 1010110 would produce output sequences 0010000 and 0010100 for block and non-block recognizers, respectively.

For block codes, the number of possible code words of length n is m^n where m is the number of symbols in the code. For the above example, *m=2* since 0 and 1 are the code characters and n=3. So the number of code words is $2^3 = 8$.

Sequential circuits can be designed as Mealy machines or Moore machines. The current output of a Mealy machine is a function of the current input and current state of the machine. Consequently, unwanted spurious outputs, or glitches, may occur if inputs change between state changes. Spurious outputs cannot occur in Moore machines since the current output is a function of only the current state. Mealy machines usually require fewer states than an equivalent Moore machine but that is preferred when spurious outputs must be avoided.

DESIGN REQUIREMENTS:

Your assignment is to design, implement, and test a recognizer/converter for converting sequences of three-bit serial binary code words to the corresponding three-bit two's complement.



Sequence Recognizer/Converter Block Diagram

1. *X* is used to input the binary code sequences to be converted.
2. *Clock* is used to tell the converter to read the current input value.
3. *Clear* is used to return the converter to its starting state.
4. *Z* is the output of the converted sequence.

PRELAB ASSIGNMENT

1. Develop the state diagram and state table for a Mealy machine that meets the specified design requirements.
2. Make a state assignment and generate state and output transition tables.
3. Derive flip-flop excitation maps. Use JK flip-flops (SN7476) for memory elements.
4. Derive a circuit output map.
5. Produce logic equations for flip-flop inputs and circuit output.
6. Capture your design using Quartus II.
7. Verify your design using Qsim (timing simulation mode).

LAB ASSIGNMENT

1. Implement your design on the DE1 using the following pin assignments.

   x = SW0 (PIN_L22)
   z = LEDR0 (PIN_R20)
   Clock = KEY0 (PIN_R22)
   Clear = SW1 (PIN_L21)

2. Test your implementation and record your results for all eight possible code words. Define any additional inputs or outputs needed to test your design.